# CONTROL OF SWITCHED DYNAMICAL SYSTEM

A Thesis submitted to Gujarat Technological University

for the Award of

**Doctor of Philosophy**

in

**Instrumentation and Control Engineering**

by

**PATEL HARDIK RASIKLAL**

**189999917009**

under supervision of

**Dr. Ankit K. Shah**


**GUJARAT TECHNOLOGICAL UNIVERSITY**
**AHMEDABAD**

[February–2024]

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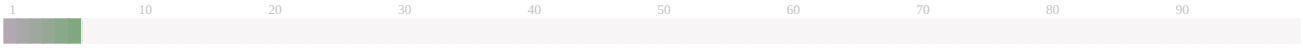


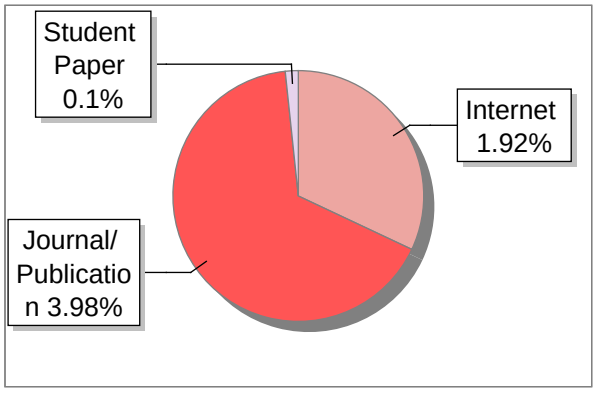


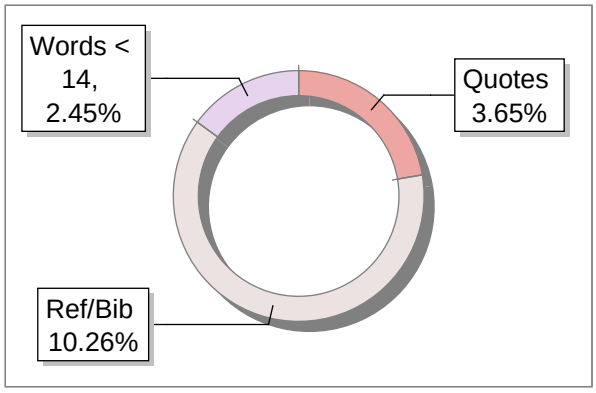


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# Abstract

This thesis delves into the realm of control theory, placing a particular emphasis on Switched Dynamical Systems (SDSs) due to their wide-ranging applicability across various fields. SDS consists of multiple subsystems or modes, each displaying distinct dynamic behaviors that are governed by a switching mechanism orchestrating transitions between these modes. The inherent complexity and mode-switching dynamics of such systems demand specialized control strategies to ensure stability, performance, and resilience. The central aim of this research is to investigate the control of SDS and explore effective techniques and algorithms for stabilizing and regulating these systems. The focus is primarily on power electronics converters such as boost and buck converters, where a boundary-based control scheme is employed. This tailored scheme is designed to regulate the output voltage, mitigate disturbances, and achieve desirable transient and steady-state performance, thereby facilitating seamless transitions between different control modes.

The study conducts a comparative assessment to gauge the efficiency of the recommended control scheme when applied to boost and buck converters. It examines various performance metrics, encompassing steady-state precision, transient behavior, resilience to disruptions, and control effort. By conducting an extensive comparison with cutting-edge techniques, this investigation offers valuable perspectives on the merits and limitations of the proposed scheme. This contribution advances comprehension of its capabilities and suitability within real-world converter systems.

Furthermore, this research directs its attention toward assessing the feasibility of the proposed control scheme by conducting an exhaustive stability analysis. Recognizing the critical importance of stability in maintaining the desired performance across diverse operational scenarios, the control design is deeply rooted in stability principles. The ensuing analysis goes a step further to scrutinize the control scheme's robustness, offering invaluable insights into its overall efficacy.

In order to assess the practical viability of the proposed control schemes, rigorous implementation experiments are carried out utilizing the FPGA-in-the-Loop (FIL) technique. This approach allows for a real-world evaluation of the proposed schemes within an FPGA-based environment. By integrating the controllers into the FPGA hardware and simulating

their performance in real-time, the FIL technique provides a robust platform to validate the effectiveness, reliability, and real-world applicability of the proposed schemes. It ensures that the control strategies can not only be theoretically designed but can also be successfully implemented and tested in hardware, ultimately confirming their feasibility for practical deployment.

In summary, the primary objective of this research is to make significant contributions to the field of control theory by exploring and developing effective control strategies for SDS, with a specific emphasis on boost and buck converters. The study encompasses a comprehensive approach, including theoretical analysis, comparative evaluations, and the practical implementation of controllers. These efforts collectively enhance comprehension and utilization of control techniques in intricate systems characterized by mode-switching dynamics.

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I would like to express my sincere appreciation and gratitude to my guide, Dr. Ankit K. Shah, for his unwavering support, guidance, and mentorship throughout this research journey. Dr. Shah's profound expertise and insightful feedback have been instrumental in shaping the direction of my research and enhancing the quality of my work. I would also like to extend my heartfelt thanks to the DPC members, Dr. Dipak M. Adhyaru and Dr. Dipesh H. Shah. Their valuable input and constructive feedback have been invaluable in refining the methodologies and approaches employed in my research. Their commitment to academic excellence and dedication to fostering a stimulating research environment have been truly inspiring.

This work would not have been possible without the constant encouragement, patience, and support of Dr. Ankit K. Shah, Dr. Dipak M. Adhyaru, and Dr. Dipesh H. Shah. I am deeply grateful for their contributions to my academic and professional growth.

Furthermore, I am deeply indebted to my parents, whose boundless love and unwavering belief in my potential have been a constant source of motivation. Their sacrifices and encouragement have been pivotal in my pursuit of knowledge.

I am deeply grateful to my wife, Anita Patel, and my son, Shubh Patel, for their steadfast and selfless support throughout my challenging Ph.D. journey. Their sacrifices and belief in me have been a constant source of strength. Whether it was late nights working on research or facing academic hurdles, their encouragement and understanding have been invaluable. Their presence has lightened my load and played a pivotal role in my academic success. I am truly fortunate to have a family that actively participates in and understands the significance of this journey. Their unwavering support has made all the difference, and for that, I am eternally thankful.

Finally, I extend my thanks to all my colleagues and friends who have supported and encouraged me throughout this challenging but rewarding journey.

**Hardik Rasiklal Patel**

# Table of Contents

# List of Abbreviations

| | |
|---|---|
| ADRC | Active Disturbance Rejection Control. |
| BC | Boundary Control. |
| CA | Circuit Averageing. |
| CCM | Continuous Conduction Mode. |
| CHIL | Controller HIL. |
| CrCM | Critical Conduction Mode. |
| DCM | Discontinuous Conduction Mode. |
| DOF | Degree of Freedom. |
| DSP | Digital Signal Processing. |
| DTC | Direct Torque Control. |
| eADRC | error-based ADRC. |
| FF | Flip Flop. |
| FIL | FPGA-in-the Loop. |
| FOPID | Fractional Order PID. |
| FPGA | Field-Programmable Gate Array. |
| GADRC | Generalized ADRC. |
| GPI-ADRC | GPI Observer-based ADRC. |
| GSSAM | Generalized State Space Average Model. |
| HADRC | Higher Control Gain ADRC. |
| HDL | Hardware Description Language. |
| HIL | Hardware-in-the-Loop. |
| IDE | Integrated Development Environment. |
| J | Gaurds. |
| LADRC | Linear ADRC. |
| LMI | Linear Matrix Inequality. |
| LTI | Linear Time-Invariant. |
| LUT | Lookup Table. |
| MADRC | Modified ADRC. |
| MBD | Model-Based Design. |
| MIL | Model-in-the-Loop. |

| | |
|---|---|
| MPC | Model Predictive Control. |
| NADRC | Filtered Derivative Feedback Control ADRC. |
| NMP | Non-Minimum Phase. |
| ODE | Ordinary Differential Equation. |
| PFM | Pulse-Frequency Modulation. |
| PID | Proportional Integral Derivative. |
| PIL | Processor-in-the-loop. |
| PWM | Pulse-Width Modulation. |
| SDS | Switched Dynamical System. |
| SIL | Software-in-the-loop. |
| SMC | Sliding Mode Control. |
| SSA | State-Space Averaging. |

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# CHAPTER-1

# Introduction

## 1.1 Background and Motivation

In the realm of engineering and science, the study of dynamic systems has remained a cornerstone for understanding the behavior of various natural and artificial phenomena. Dynamic systems are prevalent in a wide array of disciplines, ranging from mechanical and electrical engineering to biology and economics [1]. As systems grow in complexity, the need to develop efficient and robust control strategies becomes increasingly important. This has led to the emergence of a specialized area of research known as control theory, which aims to design algorithms and methodologies for governing the behavior of dynamic systems.

One class of dynamic systems that has garnered significant attention in recent years is the Switched Dynamical System (SDS) [2]. Unlike traditional continuous systems, SDS exhibit abrupt changes in their dynamics due to the presence of discrete modes or subsystems [3]. These mode transitions can be triggered by events such as switching on or off certain components, changes in environmental conditions, or shifts in system parameters.

The study of SDS holds substantial significance due to its relevance across several domains. In robotics, managing mode transitions is vital for adaptable robots. In the field of power electronics, mode transitions are of paramount importance as they directly impact the reliable operation and performance optimization of devices when they switch between modes. In the realm of biology, the dynamics of cellular processes involve mode transitions that dictate the behavior of regulatory networks, offering insights into cellular functionality.

As a result, unraveling the principles underlying SDS behavior not only enriches theoretical understanding but also paves the way for innovative applications in technology, engineering, and scientific research. SDSs provide a novel paradigm within this landscape, characterized by abrupt mode transitions. As system complexity grows, studying SDS and control theory remains essential for creating efficient strategies to manage behaviors and discover opportunities for progress.

## 1.2 Introduction to SDS

In essence, SDS refers to a type of dynamic system where the act of switching between different modes significantly influences its behavior [4] [5]. To put it more precisely, an SDS can be thought of as a two-tiered hybrid system. The first level involves various modes that are described by differential and/or difference equations, shaping the lower-level dynamics. The second level comprises a coordinator responsible for managing the transitions between these modes. This system inherently accommodates both continuous states, residing within a vector space, and discrete states, associated with specific values from a distinct index set. The interplay between these continuous and discrete states gives rise to the intricate and diverse behaviors exhibited by SDS, rendering them both highly representative and complex in nature [6].

Hybrid systems, on the other hand, combine both continuous and discrete dynamics within a unified framework. They integrate continuous dynamics, characterized by differential equations governing system behavior, with discrete dynamics, which involve abrupt changes or transitions at certain points or conditions. Hybrid systems allow for modeling complex systems with both continuous-time and discrete-event behaviors, making them more versatile for representing systems with mixed dynamics. In essence, SDSs focus on switching between different continuous dynamical modes, whereas hybrid systems encompass both continuous and discrete dynamics within a single system description.

In simple terms, imagine an SDS like a traffic controller for a complex robot. This system has two important parts: the lower level and the upper level. The lower level is like the robot's brain. It follows a set of rules (kind of like math equations) to decide what the robot should do. These rules cover things the robot can do over time, like how fast it can move or when it should stop. The upper level is like the boss of the robot. It decides when the robot should switch between different tasks. It's like the traffic controller telling the robot to go fast, slow down, or stop at certain times. Now, think of the robot as having two kinds of states. One is like its mood, which can change smoothly, like going from happy to sad. The other is like its choices, which can only be one of a few options, like picking from a menu. Because the robot's mood and choices interact, this whole setup becomes really interesting and a bit tricky to understand. These types of systems are important because they assist in controlling complex real-world phenomena, even though they can be challenging to predict.

### 1.2.1 Mathematical representation of SDS

An SDS serves as a valuable mathematical model for describing dynamic processes in which the system's behavior undergoes discrete changes triggered by specific events or conditions.

This framework encompasses multiple subsystems, each contributing to the system's behavior under certain circumstances [7]. In this section, the mathematical representation of SDS is outlined, with a focus on making the behavior of individual subsystems clear and describing the conditions that cause transitions between these subsystems.

**Subsystems and dynamics:** The core of SDS involves $m$ distinct subsystems, each characterized by a set of differential equations governing its temporal evolution. These equations encapsulate the alterations of state variables within the subsystem over time. Mathematically, it is represented for $i$-th subsystem as follows [8]:

$$\dot{x}(t) = f_i(x(t), u(t)) \tag{1.1}$$

Here:

- $i \in \{1, \ldots, m\}$, representing the $m$ subsystems in the system.
- $\dot{x}(t)$ signifies the rate of change of state variables.
- $x(t)$ represents the vector of state variables.
- $u(t)$ denotes the control input.
- $f_i$ symbolizes the function dictating how state variables evolve in response to the present state and control input within the $i$-th subsystem.

**Switching Conditions:** Essential to the SDS are the switching conditions, pivotal in determining the transitions between different subsystems. These conditions hinge on system states or predefined events. Mathematically, the switching conditions are defined as:

$$\sigma(t) = s(x(t)) \tag{1.2}$$

In this equation:

- $\sigma(t)$ designates the index of the active subsystem at time $t$, indicating the subsystem currently influencing the system's behavior.
- $s(x(t))$ is a function that selects the active subsystem based on the prevailing state $x(t)$ of the system.

**Switching Control:** To ensure seamless transitions between subsystems, a switching control strategy is employed. This strategy involves determining the control inputs for each subsystem, facilitating desired transitions. The control input $u(t)$ for the $i$-th subsystem may be influenced by both the current state $x(t)$ and the prevailing switching condition $\sigma(t)$.

**Overall System Equations:** The complete representation of the SDS manifests as a hybrid system, Ordinary Differential Equations (ODEs) and discrete transitions. The system's equations can be expressed as:

$$\dot{x}(t) = f_{\sigma(t)}(x(t), u_{\sigma(t)}(t)) \tag{1.3}$$

Within this equation:

- $\dot{x}(t)$ encompasses the vector of state variable rate changes across all subsystems.
- $f_{\sigma(t)}$ denotes the dynamics associated with the subsystem indicated by the current switching condition $\sigma(t)$.
- $u_{\sigma(t)}(t)$ represents the control input applied to the active subsystem at time $t$.

Hence, the foundation has been established through the presentation of the mathematical representation of SDS.

### 1.2.2 Classification of SDS

Instead of giving a universal formal definition for SDS, the focus is on explaining specific system categories that hold primary interest. In SDS, the events involving transitions can be systematically classified into distinct categories [6].

- State-dependent *versus* Time-dependent
- Autonomous *versus* Controlled

**State-dependent switching:** State-dependent switching within SDS involves a dynamic interplay between different subsystems, where the progression from one subsystem to another is intricately tied to the current state of the system [9]. Unlike predetermined or time-triggered transitions, state-dependent switching hinges on the values of the system's state variables at any given moment. This means that the decision to switch modes is determined by the real-time condition of the system, making it a more adaptive and context-aware process.

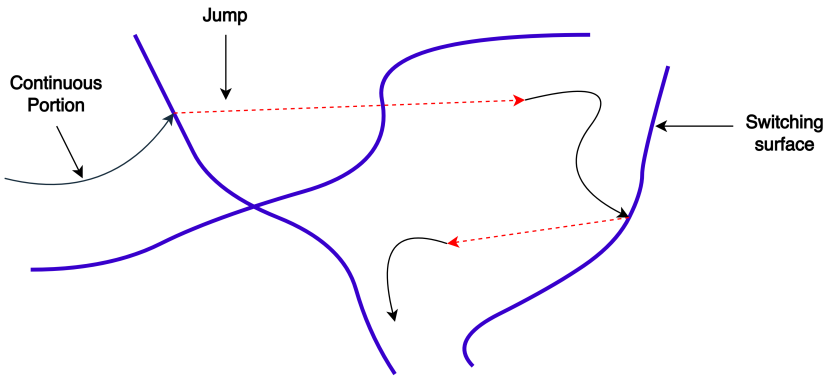



**Figure 1.1** State-dependent switching

The thick curves in Fig. 1.1 represent the switching surfaces that delineate the boundaries between subsystems [6]. When discussing state-dependent switching, these curves exemplify how the transition choices are not pre-defined but rather influenced by the state's position in relation to these surfaces. This way of switching things makes the system more interesting and complicated to control. Now, how things move and switch between modes doesn't only follow set schedules or fixed time intervals. Instead, the continuous state variables themselves guide the decision-making process, imparting a higher degree of adaptability and responsiveness to the system's dynamics.

Mathematically, consider an SDS with $m$ subsystems, where the system state is represented by $x(t) \in \mathbb{R}^m$ at time $t$. The switching condition $\sigma(t)$ is now a function of the state, denoted as $\sigma(x(t))$, determining the active subsystem. The system dynamics can be described as:

$$\dot{x}(t) = f_{\sigma(x(t))}(x(t), u_{\sigma(x(t))}(t)) \tag{1.4}$$

Here:

- $f_{\sigma(x(t))}$ represents the dynamics of the subsystem indicated by the state-dependent switching condition $\sigma(x(t))$.
- $u_{\sigma(x(t))}(t)$ is the control input associated with the active subsystem determined by $\sigma(x(t))$.

Example: Let's consider a simple state-dependent SDS that models the behavior of a vehicle [10]. The vehicle can operate in two different modes: "Cruising" and "Braking". The transition between these modes is based on the vehicle's velocity, $v(t)$.

1. Subsystem Dynamics:

- Cruising Mode (Subsystem 1): In this mode, the vehicle maintains a constant velocity.

$$\dot{v}_1(t) = 0 \tag{1.5}$$

- Braking Mode (Subsystem 2): In this mode, the vehicle applies brakes to reduce its velocity.

$$\dot{v}_2(t) = -k \cdot v_2(t) \tag{1.6}$$

  where $k$ is a positive constant indicating the braking rate.

2. Switching Condition: The switching condition, in this case, is based on the velocity:

$$\sigma(v) = \begin{cases} 1, & \text{if } v \geq v_{\text{switch}} \\ 2, & \text{if } v < v_{\text{switch}} \end{cases} \tag{1.7}$$

where $v_{\text{switch}}$ is a threshold velocity.

3. System Equations: The complete system dynamics can be written as:

$$\dot{v}(t) = \begin{cases} 0, & \text{if } v \geq v_{\text{switch}} \\ -k \cdot v(t), & \text{if } v < v_{\text{switch}} \end{cases} \tag{1.8}$$

In this example, the vehicle switches between "Cruising" and "Braking" modes based on its velocity. If the velocity is above a certain threshold, it cruises with a constant velocity; otherwise, it applies brakes to slow down. The state-dependent switching condition enhances the model's realism by capturing the effect of the vehicle's velocity on its behavior.

**Time-dependent switching:** Time-dependent switching in the context of SDSs refers to a scenario where the transition between different subsystems is triggered by predefined time intervals or specific time events [6] [11]. In other words, the decision to switch from one subsystem to another is based on the passage of time, rather than being influenced by the system's current state. This type of switching introduces a temporal aspect to the system's behavior and control. An illustration of this type of time-dependent SDS is presented in Fig. 1.2.

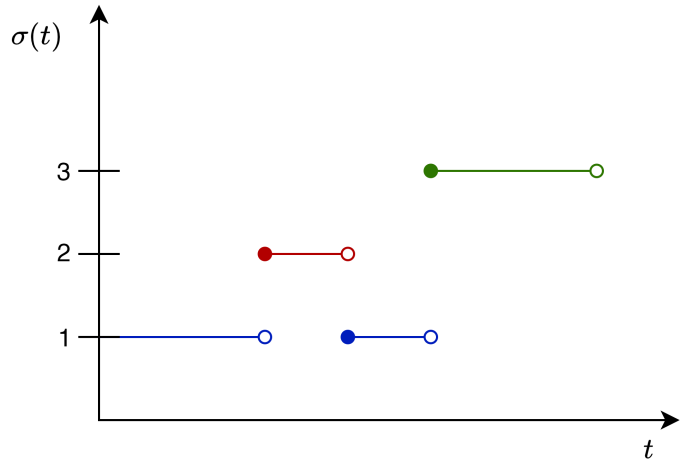



**Figure 1.2** Time-dependent switching

Mathematically, consider an SDS with $n$ subsystems. The switching condition $\sigma(t)$ is based on time, denoted as $\sigma(t) = s(t)$, where $s(t)$ is a function of time determining the active subsystem. The system dynamics can be described as:

$$\dot{x}(t) = f_{\sigma(t)}(x(t), u_{\sigma(t)}(t)) \tag{1.9}$$

Here:

- $f_{\sigma(t)}$ represents the dynamics of the subsystem indicated by the time-dependent switching condition $\sigma(t)$.

- $u_{\sigma(t)}(t)$ is the control input associated with the active subsystem determined by $\sigma(t)$.

The mathematical equations for general SDS (1.3) and time-dependent SDS (1.9) are similar, but the key distinction is in how the switching signal $\sigma(t)$ is determined.

Example: Let's consider a time-dependent SDS modeling the behavior of an automatic lighting system in a smart home. The system has two modes: "Day" mode and "Night" mode, and it switches between these modes based on predefined time intervals.

1. Subsystem Dynamics:

   - Day Mode (Subsystem 1): In this mode, the lights are off to conserve energy during the day.
   $$\dot{L}_1(t) = 0 \tag{1.10}$$

   - Night Mode (Subsystem 2): In this mode, the lights are turned on to provide illumination at night.
   $$\dot{L}_2(t) = I \tag{1.11}$$

   where $I$ is a positive constant representing the rate of increase in light intensity.

2. Switching Condition: The switching condition is based on predefined time intervals:

$$\sigma(t) = \begin{cases} 1, & \text{if time interval is day} \\ 2, & \text{if time interval is night} \end{cases} \tag{1.12}$$

3. System Equations: The complete system dynamics can be written as:

$$\dot{L}(t) = \begin{cases} 0, & \text{if time interval is day} \\ I, & \text{if time interval is night} \end{cases} \tag{1.13}$$

In this example, the lighting system switches between "Day" and "Night" modes based on predefined time intervals. During the day, the lights remain off, and during the night, they are turned on. The time-dependent switching condition in this case simplifies the decision process by relying on the passage of time rather than considering complex state variables.

Time-dependent switching is particularly useful for systems with periodic or scheduled operations where switching between different modes is driven by time-based events.

**Autonomous Switching:** Autonomous (uncontrolled) switching in the context of SDSs refers to a situation where the transitions between different subsystems occur naturally without external control inputs [12]. In other words, the switching behavior is inherent to the system's dynamics and is driven solely by the internal dynamics of the subsystems. This

type of switching doesn't involve explicit control actions from an external source, making it "autonomous."

Mathematically, consider an SDS with $m$ subsystems. The switching condition $\sigma(t)$ in the case of autonomous switching is not explicitly determined by external control inputs. Instead, it is defined by the internal dynamics of the subsystems themselves.

The system dynamics can be described as follows, and it is the most widely used equation of SDS:

$$\dot{x}(t) = f_{\sigma(t)}(x(t)) \tag{1.14}$$

Here:

- $f_{\sigma(t)}$ represents the dynamics of the subsystem indicated by the autonomous switching condition $\sigma(t)$.

Example: Let's consider an autonomous SDS representing the behavior of a chemical reaction network. The system has two chemical reactions: "Reaction 1" and "Reaction 2," and it switches between these reactions based on the concentrations of reactants and products.

1. Subsystem Dynamics:

- Reaction 1 (Subsystem 1): In this reaction, reactants $A$ and $B$ combine to form products $P$ and $Q$.

$$[\dot{A}]_1(t) = -k_1[A]_1[B]_1, \quad [\dot{B}]_1(t) = -k_1[A]_1[B]_1, \tag{1.15}$$

$$[\dot{P}]_1(t) = k_1[A]_1[B]_1, \quad [\dot{Q}]_1(t) = k_1[A]_1[B]_1, \tag{1.16}$$

  where $k_1$ is the rate constant.

- Reaction 2 (Subsystem 2): In this reaction, reactants $P$ and $Q$ react to form products $X$ and $Y$.

$$[\dot{P}]_2(t) = -k_2[P]_2[Q]_2, \quad [\dot{Q}]_2(t) = -k_2[P]_2[Q]_2, \tag{1.17}$$

$$[\dot{X}]_2(t) = k_2[P]_2[Q]_2, \quad [\dot{Y}]_2(t) = k_2[P]_2[Q]_2, \tag{1.18}$$

  where $k_2$ is the rate constant.

2. Autonomous Switching Condition: The switching between reactions is determined by the concentrations of reactants and products:

$$\sigma(t) = \begin{cases} 1, & \text{if } [A]_1[B]_1 > [P]_1[Q]_1 \\ 2, & \text{if } [A]_1[B]_1 \leq [P]_1[Q]_1 \end{cases} \tag{1.19}$$

3. System Equations: The complete system dynamics can be written as:

$$[\dot{A}](t) = \begin{cases} -k_1[A]_1[B]_1, & \text{if } \sigma(t) = 1 \\ 0, & \text{if } \sigma(t) = 2 \end{cases} \tag{1.20}$$

$$[\dot{B}](t) = \begin{cases} -k_1[A]_1[B]_1, & \text{if } \sigma(t) = 1 \\ 0, & \text{if } \sigma(t) = 2 \end{cases} \tag{1.21}$$

$$[\dot{P}](t) = \begin{cases} k_1[A]_1[B]_1 - k_2[P]_2[Q]_2, & \text{if } \sigma(t) = 1 \\ -k_2[P]_2[Q]_2, & \text{if } \sigma(t) = 2 \end{cases} \tag{1.22}$$

$$[\dot{Q}](t) = \begin{cases} k_1[A]_1[B]_1 - k_2[P]_2[Q]_2, & \text{if } \sigma(t) = 1 \\ -k_2[P]_2[Q]_2, & \text{if } \sigma(t) = 2 \end{cases} \tag{1.23}$$

$$[\dot{X}](t) = \begin{cases} 0, & \text{if } \sigma(t) = 1 \\ k_2[P]_2[Q]_2, & \text{if } \sigma(t) = 2 \end{cases} \tag{1.24}$$

$$[\dot{Y}](t) = \begin{cases} 0, & \text{if } \sigma(t) = 1 \\ k_2[P]_2[Q]_2, & \text{if } \sigma(t) = 2 \end{cases} \tag{1.25}$$

In this example, the chemical reaction network switches between "Reaction 1" and "Reaction 2" based on the concentrations of reactants and products. The switching behavior is entirely autonomous, driven by the internal dynamics of the subsystems.

Autonomous switching is often observed in natural systems where different subsystems or modes emerge spontaneously due to the underlying interactions and dynamics.

**Controlled switching:** Controlled switching in the context of SDSs refers to a scenario where the transitions between different subsystems are explicitly controlled by external inputs or a control strategy [13]. Unlike autonomous switching, where the switching behavior is intrinsic to the system's dynamics, controlled switching involves making decisions based on the system's state and possibly external factors to achieve specific objectives.

Mathematically, consider an SDS with $m$ subsystems. The switching condition $\sigma(t)$ is determined by a control law or strategy that takes into account the system's state $x(t)$, and possibly time $t$ and other external inputs. The system dynamics can be described as:

$$\dot{x}(t) = f_{\sigma(t)}(x(t), u(t)) \tag{1.26}$$

where $f_{\sigma(t)}$ represents the dynamics of the subsystem indicated by the controlled switching condition $\sigma(t)$, and $u(t)$ is the control input that influences the switching decision.

Example: Let's consider a controlled SDS modeling temperature control in a heating and cooling system [14]. The system has two modes: "Heating" and "Cooling," and it switches between these modes based on the difference between the current temperature and a desired set-point.

1. Subsystem Dynamics:

   - Heating Mode (Subsystem 1):

   $$\dot{T}_1(t) = k_1(T_{\text{set}} - T_1(t)), \tag{1.27}$$

   where $k_1$ is the heating rate constant and $T_{\text{set}}$ is the desired set-point.

   - Cooling Mode (Subsystem 2):

   $$\dot{T}_2(t) = -k_2(T_2(t) - T_{\text{set}}), \tag{1.28}$$

   where $k_2$ is the cooling rate constant.

2. Controlled Switching Condition: The switching between modes is determined by the temperature difference:

$$\sigma(t) = \begin{cases} 1, & \text{if } T_1(t) - T_{\text{set}} > T_{\text{tol}}, \\ 2, & \text{if } T_{\text{set}} - T_2(t) > T_{\text{tol}}, \end{cases} \tag{1.29}$$

where $T_{\text{tol}}$ is a tolerance representing an acceptable temperature deviation.

3. System Equations: The complete system dynamics can be written as:

$$\dot{T}(t) = \begin{cases} k_1(T_{\text{set}} - T_1(t)), & \text{if } \sigma(t) = 1, \\ -k_2(T_2(t) - T_{\text{set}}), & \text{if } \sigma(t) = 2, \end{cases} \tag{1.30}$$

where $T(t) = T_1(t) = T_2(t)$ represents the temperature.

In this example, the heating and cooling system switches between "Heating" and "Cooling" modes based on the temperature difference from the desired set-point. The controlled switching condition incorporates the control objective of maintaining the temperature close to the set-point by choosing the appropriate mode.

Controlled switching is common in systems where the choice of subsystem aims to achieve specific performance or stability goals, and external control inputs play a significant role in determining the switching behavior.

### 1.2.3 Examples of SDS

The SDSs find application in a wide range of fields where systems exhibit changing behaviors based on various conditions or modes. These examples illustrate the versatility and relevance of SDS in capturing complex dynamics across diverse domains.

- **Robotics and Autonomous Systems:** Robotic systems often encounter different environments and tasks that require adaptive behaviors. SDS is employed to enable robots to seamlessly transition between locomotion modes like walking, crawling, and flying based on terrain and obstacles [15]. For instance, drones can switch between hovering and forward flight modes to optimize energy consumption and maneuverability.

- **Energy Systems and Power Electronics:** In energy systems, SDS is instrumental in optimizing energy conversion and distribution. Renewable energy sources, such as solar and wind, employ SDS to switch between different power converter modes, such as the boost and buck types, to regulate energy flow and maximize efficiency [16]. The control strategies enable converters to adapt to variable input sources and fluctuating energy demands.

- **Transportation and Hybrid Vehicles:** Hybrid vehicles incorporate SDS to switch between power sources, such as internal combustion engines and electric motors [17]. These systems adapt to driving conditions, battery charge levels, and efficiency requirements. The control mechanisms ensure optimal power distribution, leading to improved fuel economy and reduced emissions.

- **Networked Control Systems:** Networked control systems utilize SDS to manage communication delays and uncertainties in control loops [18]. These systems switch control strategies based on real-time network conditions, ensuring accurate and timely information exchange between distributed controllers. Applications include telecommunication networks, remote robotic control, and industrial automation.

- **Chemical Reaction Networks:** Chemical systems often exhibit SDS behavior due to varying reaction rates and conditions [19]. SDS models are employed to describe how reactions switch between different pathways based on reactant concentrations, temperature, and catalyst presence. Such models aid in predicting reaction outcomes and optimizing product yields.

- **Aerospace and Flight Control:** Aerospace systems employ SDS to manage different flight phases, such as takeoff, cruising, and landing [20]. The control systems switch between control laws to optimize performance and stability under changing aerodynamic conditions. This ensures safe and efficient flight operations.

- **Manufacturing and Process Control:** Manufacturing systems use SDS to adapt to production demands and equipment availability [21]. Flexible manufacturing lines switch configurations to efficiently produce various products while minimizing downtime and setup costs. SDS models guide the decision-making process in optimizing production schedules.
- **Biological and Genetic Networks:** In biology, genetic networks exhibit SDS characteristics as genes switch on or off in response to environmental cues. These switches regulate cellular processes, development, and responses to stimuli. SDS models aid in understanding complex gene regulatory networks and their impact on cellular behavior [22].

### 1.2.4 Introduction of boost and buck-type DC-DC converters as SDS

Boost and buck-type DC-DC converters have been chosen as the focal point for an extensive study and analysis in this research endeavor. This selection is driven by their direct relevance to the field of instrumentation and control. These converters play a pivotal role in the domain of energy conversion applications, making their examination particularly pertinent to understanding dynamic system behavior in real-world scenarios. The choice is further substantiated by the inherent characteristics of these converters that align with the concept of SDS [23] [24]. Due to their inherent switching operations and mode-dependent behaviors, boost and buck converters exhibit dynamic behavior akin to SDS, thus serving as perfect examples for investigating the complexities of such systems.

The buck converter, known for its step-down voltage regulation, efficiently reduces input voltage to match desired output levels [25]. Conversely, the boost converter elevates input voltage to achieve higher output voltage [26]. Both converters operate through rapid switching of semiconductor devices, inducing nonlinearity into their dynamics. The use of the SDS framework acknowledges this nonlinearity, providing a structured approach to uncover the complex behavior that occurs when shifting between various operational modes.

Through the prism of SDS, this research reveals the underlying dynamical shifts that transpire as these converters toggle between distinctive modes. The SDS perspective facilitates insights into transient responses during mode transitions, steady-state characteristics, and the crafting of control strategies for optimal performance. Significantly, this analysis seamlessly links SDS principles with the pivotal role of instrumentation and control within energy conversion applications.

By concentrating on boost and buck-type DC-DC converters within the SDS framework, this research substantiates the pragmatic significance of SDS in the context of energy conversion. The converters' intrinsic switching dynamics harmonize naturally with SDS principles, enabling a comprehensive exploration that bridges theoretical concepts with the practical

intricacies of energy management challenges. This investigation advances not only the grasp of SDS but also offers profound insights into the indispensable role of control strategies in refining energy conversion processes.

## 1.3 Problem Statement

In the world of SDS, there's a puzzle to solve: how to manage them. These systems are like shape-shifters, always switching between different ways of behaving. This switching makes things complicated because the systems can act in weird and unpredictable ways. The big goal here is to come up with plans – let's call them control strategies – that can guide these systems. These plans need to be really smart, making sure the systems stay steady, reach their goals, and don't act too wild, even when they are switching around. So, as these systems switch from one behavior to another, these smart plans step in and keep things on track, making sure everything stays stable and goes smoothly.

Controlling SDSs involves tackling several key challenges:

- **Mode Transitions:** Figuring out how to smoothly switch between different behaviors or parts of the system while keeping everything stable and meeting performance goals.
- **Control Strategy:** Coming up with clever plans or rules that guide how the system behaves, whether it's following a particular path or meeting specific goals.
- **Stability Analysis:** Making sure the whole system stays stable both when it's switching between modes and when it's settled down in a mode.
- **Convergence:** Understanding the conditions that help the system reach a specific state or pattern without going crazy with ups and downs.
- **Robustness:** Handling uncertainties, surprises, and mistakes in the system or its plans to keep everything running smoothly.

The task of controlling SDSs is highly significant in diverse fields, including robotics, power systems, manufacturing, and autonomous vehicles. In these domains, systems frequently require the ability to adapt their operations in response to varying conditions or specific objectives.

## 1.4 Objective and Scope of Work

The main goal is to establish a comprehensive control framework that effectively manages the behavior of SDS. The project strives to create controllers capable of handling the system's shifts between different modes or parts, ensuring stability during these transitions, achieving

specific performance goals, and managing uncertainties. The ultimate objective is to forge resilient and efficient control strategies for SDS.

**Modeling SDS:**

- Develop accurate mathematical models for SDS that faithfully represent its behavior during various modes.
- Test the proposed models through simulations to check their validity and accuracy.

**Controller Design:**

- Design controllers that can handle mode changes and ensure smooth transitions between different parts of the system.

**Stability Analysis:**

- Assess the stability of the proposed control strategies to guarantee the system's stability during mode transitions and when it's operating steadily.
- Utilize tools like Lyapunov stability analysis to confirm the control system's stability.
- Assess stability in the presence of real-world complexities, such as nonlinearities, uncertainties, and varying parameters.

**Implementation:**

- Apply the designed control algorithms in simulation environments such as MATLAB/SIMULINK to confirm their effectiveness and performance.
- Evaluate the control system's performance across different scenarios, including normal operation, disturbances, and mode shifts.
- Evaluate the controller's accuracy on an Field-Programmable Gate Array (FPGA) using the Model-Based Design (MBD) method. This allows for real-time analysis, assessing the algorithm's performance and effectiveness in practical scenarios.

## 1.5 Research Contributions

The research work brings forth notable contributions, including:

- The mathematical model is formulated to incorporate mode-dependent parameters, resulting in a more faithful representation of boost and buck converters' dynamics within the context of SDS.

- Introduced an innovative control algorithm tailored to boost and buck converters, meticulously crafted to adeptly handle mode transitions. This algorithm's core objectives encompass ensuring stability, convergence, and achieving desired performance throughout the intricate process of switching operations.
- Conducted a thorough comparison that encompasses the proposed control algorithm and conventional methods like Proportional Integral Derivative (PID) and Fractional Order PID (FOPID), as well as advanced techniques like Active Disturbance Rejection Control (ADRC). This evaluation underscores the superiority of the proposed approach in terms of performance.
- The stability attributes of the boost and buck converter in the context of SDS are meticulously examined utilizing the Lyapunov method. This analytical process offers a profound comprehension of the intricate stability behavior inherent to the system.
- By leveraging MBD, the control algorithm was proficiently integrated into an Artix-7 FPGA board using the FPGA-in-the Loop (FIL) approach. This technique enabled the immediate evaluation of hardware performance for the developed control system in real-time scenarios.
- Engaging in a thoughtful exploration of potential challenges and future pathways aimed at refining and implementing the proposed control strategy in real-world systems. This discussion not only addresses practical considerations but also serves as a stepping stone for further research in this domain.
- Thus, incorporated mode-dependent parameters into a mathematical model for boost and buck converters within SDS, introduced a specialized control algorithm for smooth mode transitions ensuring stability and performance, compared with other methods, demonstrating superior performance, examined stability using Lyapunov method, and integrated control algorithm into an FPGA board for real-time evaluation.

## 1.6 Structure of the Thesis

Chapter 1 of this thesis lays the foundation by providing essential background and motivation for the research. It introduces the concept of an SDS, highlighting its significance in various applications. The chapter also delves into the rationale behind selecting boost and buck converters as focal points for the study. These converters are discussed due to their widespread use in power electronics and their role in modern energy conversion systems. By examining these converters within the context of SDS, the research aims to contribute to a deeper understanding of their dynamic behavior and control strategies, ultimately enhancing their efficiency and performance in practical applications.

In Chapter 2, an extensive literature review is presented, encompassing a diverse range of control strategies employed for the regulation of DC-DC converters. This comprehensive survey sheds light on the existing landscape of control techniques, emphasizing their strengths, weaknesses, and gaps in current knowledge. By systematically analyzing and comparing these strategies, the chapter aims to identify areas where advancements are needed. This critical examination serves as a foundation for the subsequent research, guiding the development of innovative control approaches tailored to SDSs and enhancing the robustness of DC-DC converters in various practical applications.

In Chapter 3, a comprehensive exploration of the boost converter is presented, encompassing both Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). The boost converter is modeled as an SDS, capturing its intricate dynamics. The chapter delves into the design of a tailored controller for the boost converter, encompassing its steady-state and dynamic behaviors. Through meticulous analysis, the proposed control algorithm's effectiveness is evaluated, unveiling its capability to optimize the converter's performance. The impact of parameter variations is further examined in this chapter, with a comprehensive assessment of the proposed algorithm's robustness. To demonstrate superiority, a comparative study is conducted, contrasting conventional and state-of-the-art techniques. This showcases the effectiveness of the proposed algorithm in improving transient response and overall operational stability.

In Chapter 4, an in-depth exploration of the buck converter is presented, focusing on the CCM operating mode. The buck converter is meticulously modeled as an SDS, capturing its intricate behavior. The chapter explores the design of a controller for the buck converter, encompassing its regular and varying behaviors. Through rigorous analysis, the proposed control algorithm's efficacy is evaluated, revealing its capacity to enhance the converter's overall performance. The chapter further scrutinizes the impact of parameter variations and parasitic parameters, comprehensively evaluating the robustness of the proposed algorithm. To confirm its superiority, a comparison is performed, emphasizing the excellent performance of the proposed algorithm in handling transient response and ensuring overall operational stability.

In Chapter 5, the focus shifts to stability analysis for both the boost and buck converters employing the proposed control algorithm. The chapter delves into the intricate dynamics of these converters, evaluating their stability characteristics. The assessment of stability relies on the application of multiple Lyapunov functions, a theoretical framework that provides valuable insights into the evolution of system behavior over time. This methodology helps in comprehending the dynamics of the systems and determining whether they ultimately attain stability. This comprehensive stability analysis framework provides a thorough understanding of the control algorithm's impact on the converters' stability, shedding light on their limit

cycles and long-term convergence tendencies, thus contributing to the assurance of their reliable and effective performance.

Chapter 6 thoroughly explores hardware implementation, providing a detailed account of how the designed controllers are brought to life using FPGA through the innovative FIL methodology within the MBD framework. This strategy seamlessly integrates the controller design into physical hardware, enabling real-time experimentation and evaluation. The chapter underscores FPGA technology's intrinsic flexibility, allowing dynamic adaptations and refinements to precisely match system requisites. The FIL framework demonstrates how to quickly build and refine control algorithms in a real-world context, showing that the proposed approach improves control strategies for practical uses.

In the last Chapter 7, the research concludes by summarizing the main discoveries and contributions from the study about designing and controlling boost and buck converters as SDS. The chapter reflects on the achievements and implications of the proposed control algorithm, highlighting its significance in enhancing the performance and stability of these converters. Additionally, the chapter points out possible paths for future research, highlighting areas that need more investigation and growth. By laying out these future directions, the chapter sets the stage for continued advancements in the field of power electronics, paving the way for innovative control strategies, enhanced hardware implementations, and broader applications of the SDS framework in various engineering domains.

# CHAPTER-2

# Literature Review and Methodology

To start this study, the chapter begins by conducting a detailed review of recent literature related to the subject. Since DC-DC converters serve as illustrative instances of SDSs, a greater emphasis is placed on them in the literature review. This review succinctly captures the essence of existing research, while also pinpointing gaps and discrepancies that the current study aims to tackle head-on. At the same time, the methodology section becomes the focus, carefully explaining the strategies and methods used to collect and analyze the information.

## 2.1 Literature Review on Modeling of SDS

In SDS modeling, a fundamental approach involves utilizing state-space formulations. This approach integrates state-space analysis with small-signal models, large-signal models, and Circuit Averageing (CA) techniques to extract crucial system characteristics for effective control strategy design. This methodology enables analyzing system behavior around an operating point and simplifying complex nonlinear dynamics.

A simpler small-signal model for a buck converter is shown using the CA method. This model helps understand how the converter works and its transfer functions without needing complicated matrix math like in the State-Space Averaging (SSA) with parasitic elements [27]. Additionally, an advanced averaged small-signal model for Pulse-Width Modulation (PWM) DC-DC converters is introduced, accounting for non-negligible transistor switching losses [28]. State-space averaged models of current-mode controlled converters are derived for buck, boost, and flyback topologies operating in CCM, enabling simplified and accurate modeling while integrating modern control techniques [29]. Furthermore, a novel Generalized State Space Average Model (GSSAM) is tailored for multi-phase interleaved converters, capable of capturing complex current and voltage switching behavior, catering to converters with oscillatory behavior, validated against a detailed switching model, and adaptable to various phase numbers for comprehensive switching dynamics representation [30]. However, simulation results indicate that neglecting the inductor parasitic resistance renders both GSSAM and the conventional average model inadequate in representing switching dynamics.

A large-signal non-ideal averaged model of a PWM DC-DC boost converter is realized using MATLAB s-function. This model features voltage-mode control with a type III compensator to enhance system response and stability. The model's validation is performed through simulations, assessing tracking performance and stability under changing conditions [31]. Moreover, SSA and CA modeling methods for DC-DC converters in DCM are examined. This exploration reveals the variability of their small-signal transfer functions and presents a selection strategy for high-accuracy modeling, crucial for designing accurate DCM closed-loop controllers to achieve enhanced stability and transient response [32].

It's important to note that while small-signal modeling provides linear approximations for stability analysis, it may not accurately represent system behavior during large disturbances [33]. On the other hand, large-signal modeling offers a more accurate portrayal of system behavior under extreme conditions but can be complex due to nonlinear terms [33]. CA techniques simplify converters into continuous-time circuits for more manageable analysis, yet they might lead to a loss of detailed dynamics and limited accuracy. A notable gap exists in accurately representing DCM in converter modeling, impacting control strategy design for this mode [28] [29] [31]. This gap underscores the need for comprehensive modeling approaches that cover both CCM and DCM, ensuring accurate predictions across various operational conditions.

## 2.2 Literature Review on Control Strategies of SDS

In the realm of SDSs and technological advancements, the efficacy of control strategies stands as a pivotal cornerstone. By analyzing a range of works, this review seeks to shed light on the evolution, challenges, and promising directions within the realm of control strategies.

In the field of control strategies, there are many classifications, each providing unique viewpoints on the complexities of this area. Within the scope of this research, a comprehensive categorization pertinent to the study's theme has been pursued. This undertaking seeks to establish a holistic framework that facilitates a thorough comprehension of the subject matter. Such an approach facilitates a concentrated examination of control strategies, thereby enabling a more profound scrutiny of the fundamental principles and practical applications that underlie them. This categorization approach facilitates a more refined exploration of the diverse facets within the field, leading to a deeper understanding of the control of SDSs and the complexities associated with it.

### 2.2.1 Conventional control

In the domain of controlling SDS, a commonly suggested approach involves the utilization of established controllers, such as the PID controller [34] [35]. This controller regulates the converter's duty cycle by evaluating the difference between the target output and the actual output, making it relatively straightforward to implement. However, the process of fine-tuning these controllers often entails a substantial investment of time and a series of trial-and-error iterations. To enhance the performance of DC-DC converters, several adaptations and refinements to PID control have been proposed.

In this context, FOPID controllers emerge as an advancement beyond conventional PID controllers, demonstrating heightened control efficacy [36] [37]. A Lyapunov-based adaptive PID strategy is presented aimed at enhancing stability, robustness, and wide disturbance rejection in DC-DC buck converter, as compared to conventional PID control [38]. While PID control presents simplicity in implementation, its effectiveness can be limited when confronted with varying operational conditions or nonlinearities within the system. Hence, the search for the best control strategies goes beyond the simplicity of PID, encouraging the exploration of more advanced methodologies to secure robust performance in the face of diverse and complex dynamics.

### 2.2.2 Control strategies for challenging phase behavior

Among DC-DC boost and buck converters, the boost converter demonstrates Non-Minimum Phase (NMP) behavior due to the dynamic shift of its positive zero location [39] [40]. This phenomenon introduces challenges in stability and control design, posing a significant obstacle to achieving the intended closed-loop bandwidth through feedback control [41]. The complex movement of the positive zero in response to changes in converter parameters worsens this challenge, sometimes causing instability. A novel approach to robust PID controller design, employing a modified direct synthesis methodology, has been put forth to address the challenge of mitigating disturbances in a NMP DC-DC boost converter operating within CCM [42].

Researchers employ ADRC, using extended state observers, to mitigate NMP issues [43]. Accurate models are vital for effective disturbance rejection, as parameter fluctuations can hinder ADRC's performance. The introduction of Model Predictive Control (MPC) for addressing NMP behavior has also brought about an increase in the response time of the controller due to the high computational burden resulting from the utilization of long prediction horizons [44]. A sliding mode backstepping controller is proposed to address the instability caused by the NMP nature of the boost converter, achieving asymptotic stability by indirectly controlling the output voltage through the sliding surface [45].

### 2.2.3 Boundary control

Boundary Control (BC) is a control strategy that aims to manage the behavior of the system through a geometric approach. Traditionally, this was done using analog circuits, but there is a growing trend towards using digital control methods [46] [47]. However, for digital control to work effectively, it requires fast measurements of voltage and current, which in turn need high sampling rates and powerful processors. This can be a challenge, especially in high-frequency DC-DC converters. Geometric controls offer the advantage of quick response times, but relying solely on simple linear boundary-based solutions might not always yield the best results [33]. Moreover, it's important to keep in mind that real-world factors like variations in components and unexpected properties in the system can significantly affect how the system behaves when dealing with larger changes in input and load conditions [48]. An adaptive Sliding Mode Control (SMC) with boundary estimation algorithm is presented that enhances control performance and robustness in discontinuous dynamical systems with uncertain physical switching boundaries [49]. However, the reliance on modeling and estimation could lead to inaccuracies in describing the discontinuous physical properties of control actuators, potentially causing mismatches between subsystems and controllers. The incorporation of a second-order switching surface for boundary control in buck converters enhances steady-state and transient behaviors, expediting trajectory movement toward the target operating point; nonetheless, the examination of its applicability to the discontinuous mode was not pursued [50].

Finally, it's important to mention that these control methods require many complicated calculations. So, even though the concept of using BC to control converters might sound simple, putting it into practice involves addressing various difficulties and complexities.

### 2.2.4 Hybrid system approach

The control of SDSs often approached as a hybrid system, integrating continuous and discrete control strategies to manage the complexities of mode-switching dynamics. The finite-time stability analysis for general dynamical systems is presented under an event-triggered control mechanism, with derived sufficient finite-time stability criteria and simultaneous exclusion of zeno behavior, demonstrated through effective finite-time stabilization and synchronization of chaotic systems in typical numerical examples [51]. A hybrid control strategy for stabilizing a class of nonlinear switched systems using a mixed H∞ and passivity performance index is proposed, offering a unified framework for solving both control problems. However, the approach necessitates solving a set of Linear Matrix Inequality (LMI) to design the hybrid controllers, potentially resulting in computational complexity and heightened implementation

effort [52]. A concise overview of optimal control methods for switched systems is provided by the survey, encompassing various problem classes and methodologies, including the summarization of computational results and available software packages [53]. An efficient and systematic approach to designing switched linear control systems with average dwell time is provided by the hybrid control scheme, wherein boundary conditions can be incorporated into the synthesis problem through convex formulation, allowing for the attainment of stability and optimal performance [54]. The problem of hybrid modeling and control of a fixed-frequency DC-DC converter, specifically the non-inverting buck-boost converter, with accurate control achieved through the utilization of MPC and explicit solution derivation. However, the need arises to approximate nonlinear terms using piecewise affine approximation in the process, which could introduce errors in the model accuracy [55].

In another investigation, the integration of hybrid automata into MBD frameworks for cyber-physical systems was examined. This strategy's validation was demonstrated on a closed-loop buck converter [56]. However, a drawback was identified: the use of a relaxation parameter during the translation process, which had the potential to cause either an under-approximation or an over-approximation of hybrid automaton trajectories, depending on its value. An energy balance-based hybrid control [57] and hybrid control based on Pulse-Frequency Modulation (PFM) + Sinusoidal PWM [58] are presented; however, their applicability is confined to DCM operation. An exact model was utilized for controller design within a large signal hybrid automaton representing a boost converter, effectively addressing voltage regulation challenges while contending with computational complexity and a high switching frequency [59]. In an extension of this work, an algorithm incorporating hybrid control is implemented, although it doesn't assure a consistent switching frequency, thereby presenting challenges for effective filtering [60]. Another technique introduced a switched linear system model to analyze the controllability of nonlinear high-order DC-DC converters [61]. However, it was observed that this method could lead to uncontrollability in situations where state variables possessed direct relationships due to the physical circuit attributes. Furthermore, the modeling didn't extensively consider parasitic parameters of electronic components, which could impact other converters. A framework was also presented to identify and validate affine hybrid automata using input-output traces [62]. However, a drawback was its reliance on the availability and precision of input and output traces, which might not always be accessible. Moreover, imperfections in ODEs estimations and the clustering method used for trace segmentation could lead to errors in the resulting automaton.

Notably, most of these approaches involve a high level of complexity and necessitate substantial mathematical computations.

## 2.3 Literature Review on Stability Analysis of SDS

In the field of SDS, ensuring stability is of utmost importance as it greatly impacts the performance and dependability of systems. This literature review begins an investigation into stability analysis in the context of SDS, with the goal of uncovering the complex relationship between switching behaviors and system stability. By examining various studies, this review aims to offer a complete summary of methods, theories, and practical uses that enhance comprehension of stability in this dynamic field.

Stability analysis of SDSs involves investigating the conditions under which the system's trajectories remain bounded over time. This analysis is more intricate than that of traditional continuous or discrete systems due to the interaction between subsystems and the switching mechanism. Key concepts in the stability analysis of SDSs include dwell time, common Lyapunov functions, and the notions of multiple Lyapunov-like functions to capture various modes of system behavior.

Lyapunov-based methods are fundamental approaches used to analyze the stability of SDS. These methods leverage Lyapunov functions, which are scalar functions that capture the system's energy or "distance" from an equilibrium point. The central idea is to find a Lyapunov function that guarantees the stability of each subsystem and then combine these functions to ensure the stability of the entire switched system.

Utilizing a multiple Lyapunov approach emerges as one method for stability analysis within switched and hybrid systems, presenting a less conservative stability analysis approach [63] [64]. This approach is presented for switched systems using multiple Lyapunov functions, accommodating varying states and potential lack of shared equilibrium points or unstable subsystems while ensuring both Lyapunov and asymptotic stability [65]. Additionally, a comprehensive framework is provided for analyzing the stability of nonlinear switched systems. This framework incorporates the method of multiple Lyapunov functions and adapted comparison principles for both deterministic and stochastic cases [66]. Furthermore, the problem of stability analysis and control synthesis for discrete-time switched systems is addressed. This is achieved by employing switched quadratic Lyapunov functions and two equivalent LMI-based conditions [67].

Moreover, researchers have introduced various modified Lyapunov methods in the field. For instance, they have proposed the utilization of multiple discontinuous convex Lyapunov functions for continuous-time switched systems [68]. In the context of discrete-time switched systems, a strategy involving multiple piecewise convex Lyapunov functions has been presented [69]. Additionally, the concept of predictive Lyapunov functions has been put forward for discrete-time switched systems [70]. Moreover, an enhanced approach involving improved

multiple Lyapunov functions has been introduced for dealing with the stability analysis of nonlinear switched systems [71]. These innovative techniques expand the analytical toolbox for addressing stability challenges in diverse switched system scenarios.

## 2.4 Literature Review on MBD Approach

MBD is a structured method that uses simulation to deeply comprehend the complex behaviors of either an upcoming or an already existing physical system. This methodology revolves around the creation of software-based models, which serve as virtual counterparts to the diverse components within the physical system under scrutiny [72]. These models extend their reach across a broad spectrum of energy-conserving domains, encompassing realms such as electrical, mechanical, thermal, hydraulic, pneumatic, and optical aspects, either independently or in intricate combinations [73].

Researchers have employed MBD through FIL setups to verify the effectiveness of control algorithms in their studies. A basic example of an electronic power system is depicted through the utilization of FIL. This demonstration highlights an industrial application in which a DC-DC buck converter, adjusted with a PID controller, is employed [74]. Similarly, ARM Cortex M4 with MATLAB serves as a versatile platform for a wide range of power electronics experiments and applications, offering flexibility and cost-effectiveness in its customization [75]. Additionally, an innovative non-linear SMC method is presented to enhance energy generation and quality in a wind energy system. The effectiveness of this technique is confirmed through co-simulation using FIL, leading to improved robustness and efficiency [76]. Moreover, A hysteresis-based Direct Torque Control (DTC) of a three-phase induction motor was experimentally conducted, and the DTC algorithm was also modeled in a hardware environment using FIL feature, showing comparable results between experimental and FPGA-based hardware simulation [77].

Overall, MBD offers several benefits, including reduced development time, improved product quality, enhanced system understanding, and efficient design iteration [78]. However, it also requires specialized tools and expertise to effectively create and manage the models, as well as to integrate the models into the final product.

## 2.5 Proposed Methodology

By exploring the difficulties linked to different modeling and control strategies mentioned earlier, this study introduces a new approach. The primary objective of this approach is to address these challenges while minimizing the need for complex mathematical computations. The central focus of this methodology is to devise a comprehensive strategy for effectively

controlling switching DC-DC converters, with a specific emphasis on their application to DC-DC boost and buck converters.

To comprehensively address the challenges presented in this study, a thorough modeling process is carried out using a hybrid automaton approach. This advanced modeling technique doesn't just capture the continuous movements of the converters; it also accurately represents the abrupt changes that happen as the system switches between different operational modes. By treating the DC-DC boost and buck converters as SDS, the research capitalizes on their inherent mode-switching behavior during operation. This behavior, inherent to such converters, demands an approach that can seamlessly handle both continuous and discrete dynamics. The chosen methodology, the hybrid automaton framework, adeptly combines these aspects, providing a comprehensive grasp of the converters' intricate behaviors across various operational conditions.

In this methodology, PWM control is implemented for CCM, and PFM is chosen for DCM operation. Both CCM and DCM are considered for boost converter, whereas for buck converter, only CCM is considered. In CCM, there are two states, and in DCM, there are three states, typically known as modes. These modes result from the switching of components in the converter. The choice of PWM for CCM ensures a consistent switching frequency, making subsequent filtering more straightforward, unlike the situation in [60]. PWM represents a widely utilized technique for controlling DC-DC converters. Nevertheless, it can lead to undesired switching losses under light load conditions. To address this concern, the approach seamlessly transitions to PFM during light loads, effectively reducing switching losses [79]. However, the complexity of filter design is notably heightened when implementing the PFM technique as opposed to the more conventional PWM. This is primarily due to the inherently variable switching frequency characteristic of PFM. Unlike PWM, where the switching frequency remains relatively constant, PFM adjusts the switching frequency based on load conditions. This dynamic behavior introduces additional challenges in designing effective filters capable of adequately attenuating the variable-frequency noise, making PFM-based converter designs a more intricate task in terms of noise management and filtering strategies. In totality, this dual control strategy for boost converters proves beneficial, especially in situations characterized by fluctuating load conditions.

To achieve controlled and optimized switching between the diverse modes of operation, the research methodically defines operational boundaries. These boundaries play a crucial role in determining the conditions under which the system transitions from one mode to another. Essential parameters like input and output voltages, current levels, and load characteristics are used as the foundation for establishing these boundaries. This precise distinction is crucial for preventing unpredictable switching and ensuring that the converters function within stable and desired areas. By implementing these precise boundaries, the control strategy can be

fine-tuned to ensure not only seamless mode transitions but also to prevent any undesired transient effects that could otherwise compromise the system's efficiency and stability.

Following the formulation of the control strategy, a thorough stability analysis is conducted. Subsequently, the implementation of the controller is accomplished through the utilization of FIL technique. Fig. 2.1 visually represents the overall process and its operational characteristics. This approach involves the application of FPGA technology to emulate and validate the controller's performance within a real-time environment. The incorporation of FPGA within the control loop ensures the validation of both the theoretical soundness and practical feasibility of the methodology.

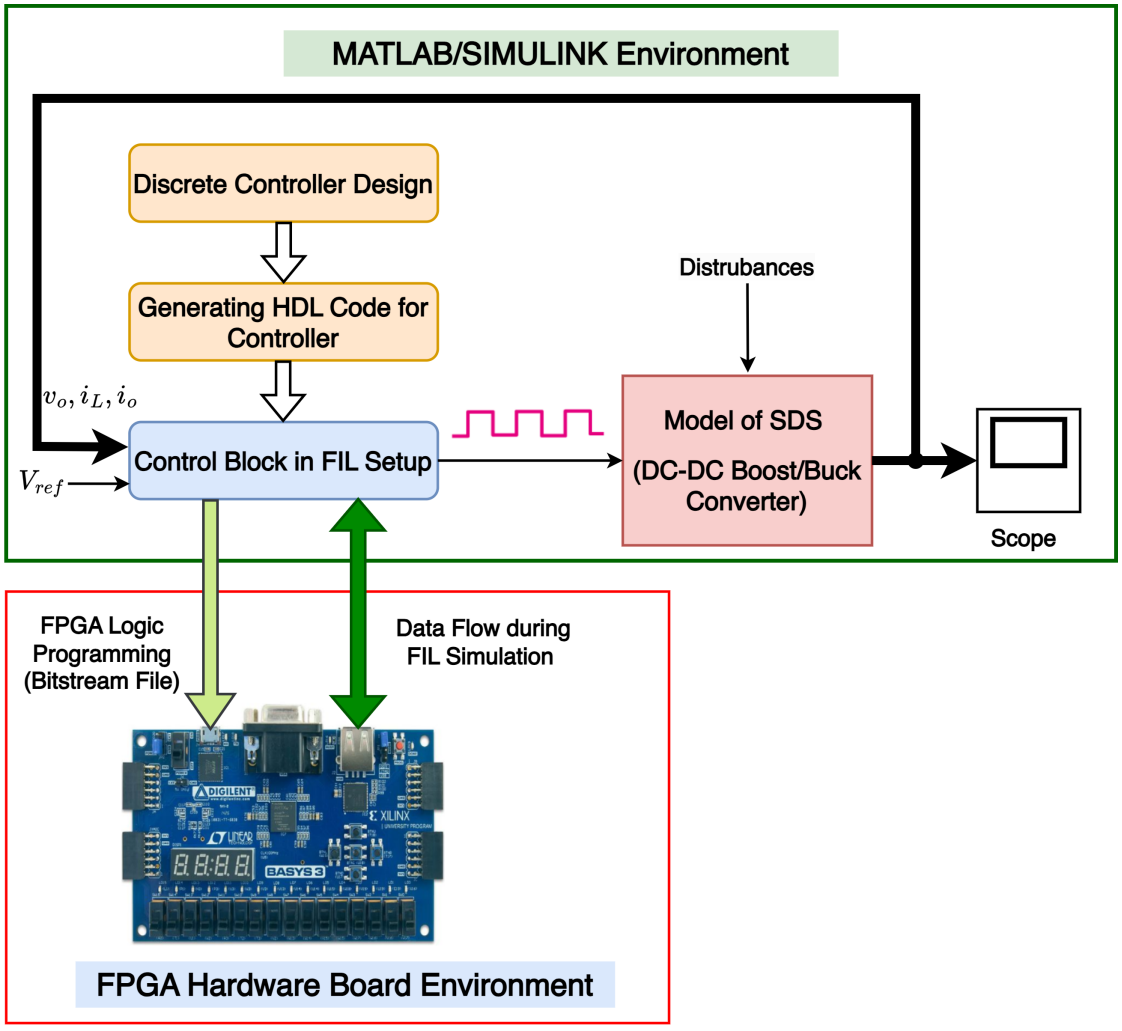



**Figure 2.1** Methodology of the proposed design approach

To sum up, this approach aims to bridge the gap between theoretical concepts and practical implementation, facilitating the creation of more effective strategies for controlling SDS. It aims to provide a comprehensive and efficient solution to the issues related to modeling and managing SDS, particularly in the context of DC-DC converters.

## 2.6 Summary

The literature on SDS emphasizes the significance of diverse modeling methods, including state-space representations, small-signal, and large-signal models. These approaches collectively capture mode transitions, stability analysis, and system nonlinearity. Control strategies, ranging from traditional PID control to ADRC and BC, are studied. Hybrid systems integrating discrete and continuous control methods show promise in managing switched system complexities.

Stability analysis, especially using Lyapunov functions, is crucial, ensuring stability in modes and transitions. Limit cycle stability analysis provides insights into periodic behaviors in SDSs. MBD transforms engineering and control systems. It offers a systematic framework for controller design and implementation. Various MBD techniques are explored, including the use of FIL for testing and validating control strategies. A concise overview of the proposed methodology highlights its core aspects, emphasizing its realization through FIL.

# CHAPTER-3

# Control of DC-DC Boost Converter

As renewable energy sources gain significance and portable devices continue to proliferate, the demand for consistent voltage and improved energy utilization becomes more pronounced [80]. This chapter delves into the realm of DC-DC boost converter control, aiming to simplify the understanding of their functionality. The exploration commences by examining the fundamental operations of the boost converter and operational strategies. The attention subsequently turns to model the boost converter, where the utilization of a technique known as SDS and hybrid automaton takes the place of intricate models. This approach yields a more precise depiction of the converter's behavior, encompassing its evolving patterns and specific control actions. This innovative technique facilitates a comprehensive grasp of DC-DC boost converter control, unlocking avenues for enhanced efficiency and reliability across various energy requirements.

## 3.1 Fundamental Insights into Boost Converter Operation

A boost converter is a type of DC-DC power converter used to step up (increase) the output voltage from a DC source. It's widely used in various applications, including power supplies, battery chargers, and renewable energy systems [81]. The basic principle of a boost converter involves the use of an inductor, a switching element (typically a transistor), a diode, and a capacitor as shown in Fig. 3.1 [82]. While ideal components are assumed for analysis, the preceding section addresses the incorporation of parametric variations to account for real-world conditions.

The fundamental operation of the boost converter can be described as follows:

- **Inductor charging (On-state):** When the switching transistor is turned on (conducting), current flows from the input source through the inductor and the transistor to the ground. The inductor resists sudden changes in current, causing it to store energy in the form of a magnetic field.
- **Inductor discharging (Off-state):** When the switching transistor is turned off (non-

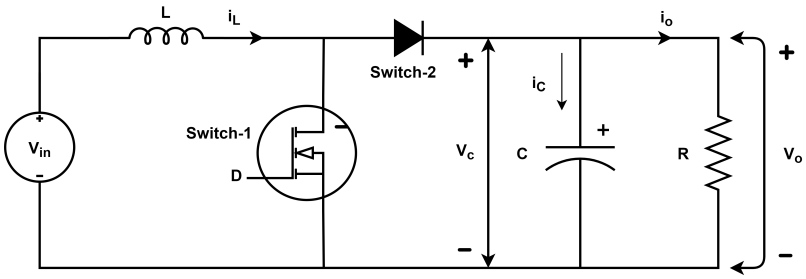



**Figure 3.1** Typical switched boost converter circuit diagram

conducting), the current through the inductor cannot instantaneously change. The inductor's stored energy generates a voltage across its terminals, trying to maintain the current flow. This causes the voltage across the inductor to rise and become higher than the input voltage.

- **Diode action:** The voltage across the inductor becomes higher than the input voltage, and this causes the diode to become forward-biased. The diode allows the inductor current to continue flowing, but it prevents the current from flowing back into the input source.
- **Output capacitor usage:** The current flows through the diode and charges the output capacitor, increasing the output voltage. The capacitor smooths out the voltage ripple, providing a more stable output.
- **Regulation:** To regulate the output voltage, a feedback control loop can be used. This involves measuring the output voltage and adjusting the duty cycle of the switching transistor based on the difference between the desired output voltage and the actual measured voltage.
- **Continuous vs. Discontinuous mode:** The boost converter can operate in continuous or discontinuous modes, depending on the relationship between the load current and the inductor current. In CCM, the inductor current never reaches zero during the switching cycle. In DCM, the inductor current drops to zero before the next cycle starts.

## 3.2 Modeling of Boost Converter

The focus is on creating an accurate representation of the boost converter's behavior within the framework of SDS. This involves formulating mathematical equations that capture the relationships between key variables, such as input voltage, output voltage, inductor current, and switch positions. By employing the principles of SDS, the modeling process aims to capture the dynamic changes that occur during switching transitions, providing insights into the converter's transient and steady-state behaviors. This thorough examination enhances

the understanding of how the boost converter operates and opens opportunities for improved control strategies within the SDS framework. Table 3.1 presents the notation utilized for the purpose of analysis.

**Table 3.1** The list of symbols and notations

| Symbol | Description |
|---|---|
| Switch-1 | MOSFET |
| Switch-2 | Diode |
| $f$ | Switching frequency of MOSFET |
| $D$ | Duty cycle |
| $V_{in}$ | Input voltage |
| $V_{ref}$ | Reference or Set-point voltage |
| $V_L$ | Voltage across inductor |
| $i_c$ | Instantaneous capacitor current |
| $i_L$ | Instantaneous inductor current |
| $I_L$ | Average value of inductor current |
| $\Delta i_L$ | Ripple in inductor current |
| $I_{UP}$ | Upper peak value of $i_L$ |
| $I_{LP}$ | Lower peak value of $i_L$ |
| $V_C$ | Average voltage across capacitor |
| $v_o$ | Instantaneous output voltage |
| $V_o$ | Average output voltage |
| $\Delta v_o$ | Output voltage swing |
| $M_p$ | Peak overshoot |
| $T_s$ | Settling time |

### 3.2.1 State-space modeling of boost converter

Let $X \in R^n$ be the continuous state and $k$ takes values in finite set $K = \{1, \ldots, N\}$ and is discrete state represents the on/off configuration of MOSFET and diode. For each $k \in K$, continuous dynamics is modeled by the differential equation as below [59]:

$$\dot{x}(t) = A_k x(t) + B_k \tag{3.1}$$

Where $x \in X$ is state vector, $A_k \in R^{n \times n}$ is system matrix and $B_k \in R^{n \times 1}$.

The inclusion of two switches within the circuit allows for distinct states to be achieved. In this context, the analysis of the boost converter involves the consideration of inductor current and output voltage as state variables. As a result, the second-order switched boost converter

encompasses a total of four discrete states. Each state corresponds to a unique state matrix, outlined in Table 3.2. The diagram in Fig. 3.2 further elucidates the circuit configuration for each of these states [83]. Notably, the discrete state $k_3$ is associated with DCM, and $k_4$ is considered infeasible; hence, these particular circuits are not depicted.

**Table 3.2** Boost converter possible discrete state and corresponding system state matrices

| Operating mode ($K_i$) | Switch-1 | Switch-2 | $A_i$ | $B_i$ |
|---|---|---|---|---|
| $k_1$ | ON | OFF | $\begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix}$ | $\begin{bmatrix} \frac{V_{in}}{L} \\ 0 \end{bmatrix}$ |
| $k_2$ | OFF | ON | $\begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}$ | $\begin{bmatrix} \frac{V_{in}}{L} \\ 0 \end{bmatrix}$ |
| $k_3$ | OFF | OFF | $\begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix}$ | $\begin{bmatrix} 0 \\ 0 \end{bmatrix}$ |
| $k_4$ | ON | ON | Impractical | |

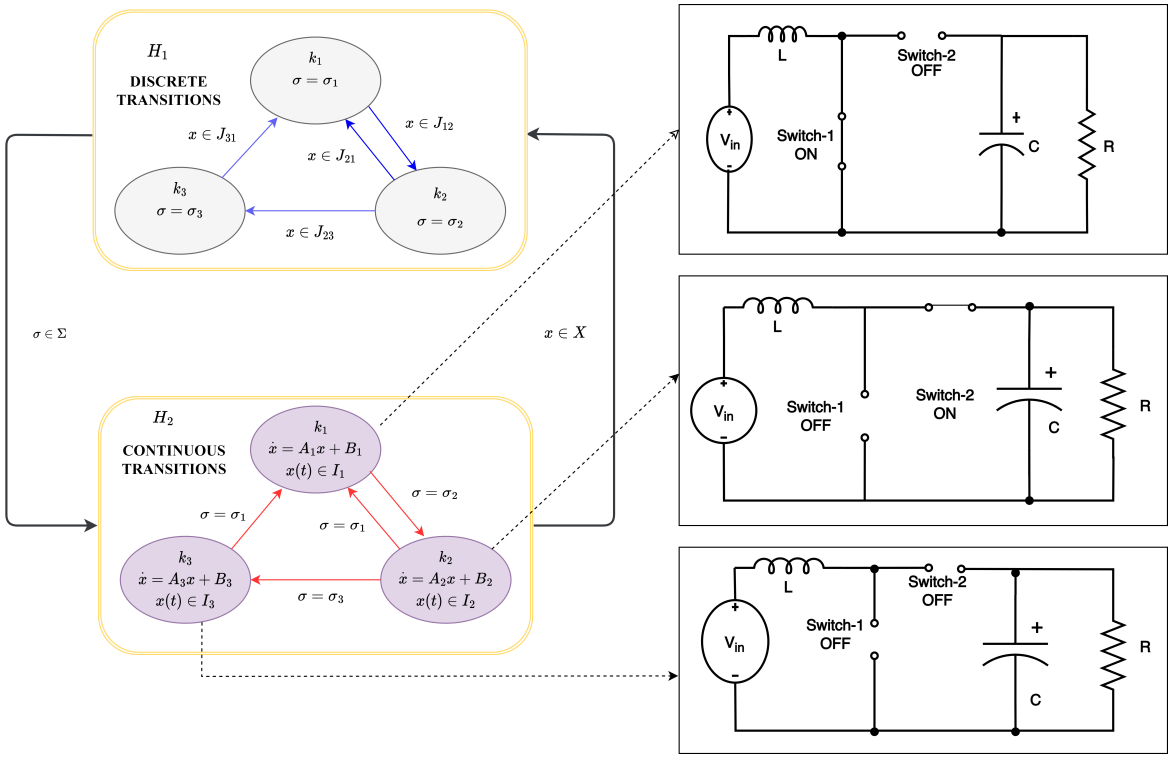



**Figure 3.2** Hybrid automaton representation of DC-DC boost converter for CCM and DCM: Interplay between continuous and discrete transitions with mode circuits

### 3.2.2 Hybrid automaton representation of boost converter

The SDS represents a distinctive category within hybrid systems and is mathematically described by [84] [85],

$$\dot{x}(t) = f_\sigma(x(t)) \tag{3.2}$$

Where $x(t)$ is the state of the system at time $t$, $\dot{x}(t) = f_\sigma(x(t))$ is the state-transition function, which describes the dynamics of the system in the $\sigma$ mode of operation. The operation of the system is determined by a switching signal $\sigma$ that is defined by a set of state-dependent boundaries. Here, $\sigma$ is taking values from index set $M = \{1, ..., m\}$ and $m$ represents the number of subsystems. When the system's state crosses a boundary, a transition occurs, causing the system to shift into a new mode of operation. Each mode is characterized by specific state-transition functions that are triggered by the corresponding boundaries.

The DC-DC converter embodies a blend of continuous and discrete behaviors through its use of passive components and switches. This interplay can be illustrated as a hybrid automaton, as depicted in Fig. 3.2. A hybrid automaton, represented by the tuple $\mathcal{H} = \{K, X, F, I, E, g, J\}$, encapsulates the following elements [83]:

- $K = \{k_1, k_2, k_3\}$ is a finite set of topologies that represent the possible states of the converter. Here, it includes the topology where the switch is closed (charging the inductor) and the topology where the switch is open (discharging the inductor).
- $X$ - continuous state of the system and it is defined by $(k, x) \in K \times X$ : inductor current and output voltage.
- A state is defined by $F : (K \times X) \rightarrow R^n$ is a vector field.
- $I : K \rightarrow 2^X$ is a mapping that assigns an invariant set $I_k \subseteq X$ for each topology $k \in K$.
- $E \subseteq (K \times K)$ is a set of feasible discrete transitions (or events) allowed among the topologies. Here, the transition from the charging topology to the discharging topology and vice versa.
- $g : E \rightarrow J$ is the guard function. It determines when a discrete transition is feasible. For example, a guard function is used to ensure that the switch is only closed when the voltage across the inductor is below a certain threshold.
- $Gaurds(J)$: $J \subseteq 2^X$ is the guard that determines the effect of a discrete transition on the continuous state $X$ . Here when the switch is closed, the inductor will charge and the voltage across it will increase, while when the switch is open, the inductor will discharge and the voltage across it will decrease.

In Fig. 3.2, $H_1$ and $H_2$ denote two distinct transition types, where $H_1$ represents a discrete transition and $H_2$ signifies a continuous one. The occurrence of a $H_1$ transition relies on the continuous signal $x$ originating from $H_2$, while the $H_2$ transition takes in a discrete value $\sigma \in \Sigma$ from $H_1$. Subsequently, the continuous state $x$ evolves in response to this $H_2$ transition.

## 3.3 Development of Boost Converter Control Strategies

Here, the boost converter is represented as an SDS using a hybrid automaton. One of the main design challenges involves determining the suitable $J$ for both CCM and DCM modes. These $J$ hold significant importance as they are chosen deliberately based on system dynamics and control objectives. Their careful selection ensures smooth transitions and affects the system's stability and robustness. The proper choice of the $J$ is instrumental in maintaining state trajectories within acceptable limits. Notably, the only distinction between CCM and DCM operations is the absence of $J_{31}$ in CCM. The proposed algorithm put forth utilizes PWM and PFM control strategies for CCM and DCM operations, respectively. When the load is light and the control mechanism shifts to PFM, it leads to a reduction in switching and driver losses owing to the decreased switching frequency [86]. The outcome of this design is depicted in Fig. 3.3, illustrating the resulting closed-loop hybrid control scheme.

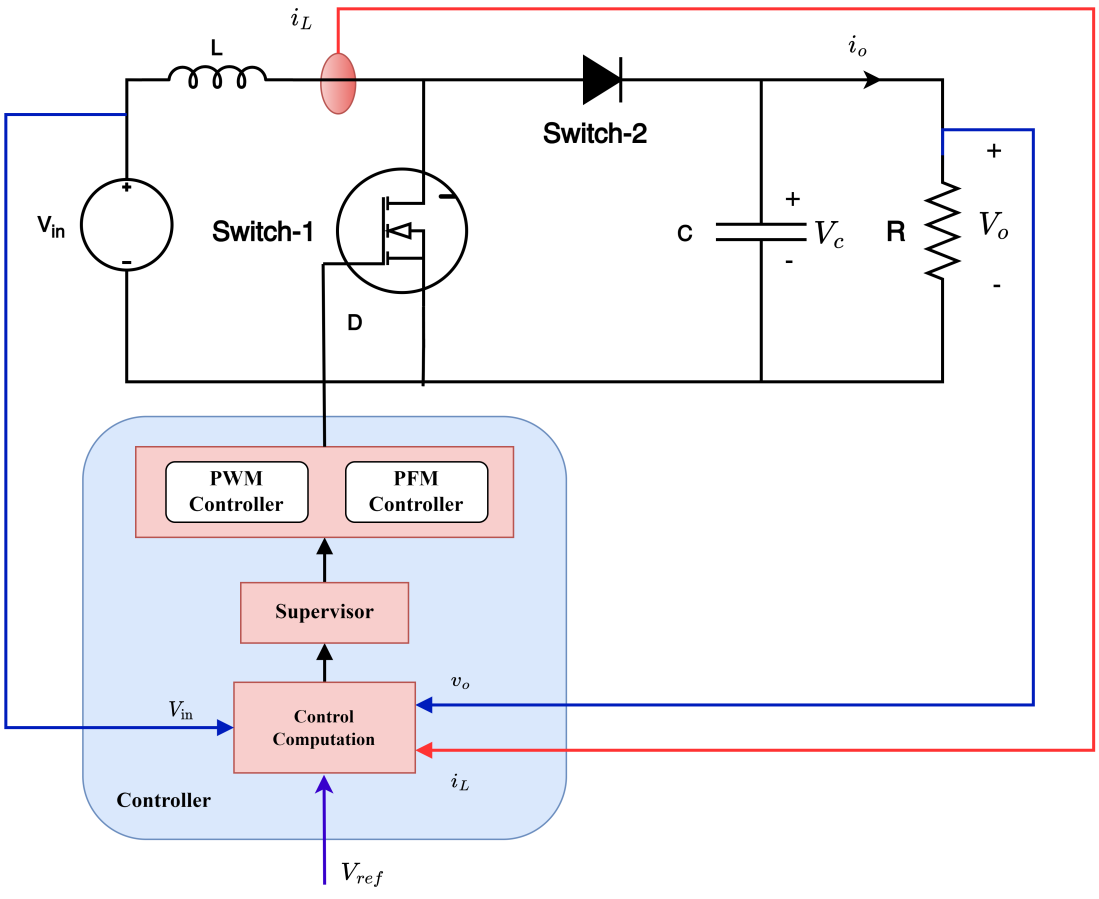



**Figure 3.3** The proposed closed-loop control scheme for boost converter

### 3.3.1 PWM controller design for CCM

Fig. 3.4 presents approximated waveforms depicting the inductor current and output voltage of a switched boost converter operating in CCM. Here, the selection of $J$ is crucial to ensure the implementation of a fixed-frequency PWM control scheme.

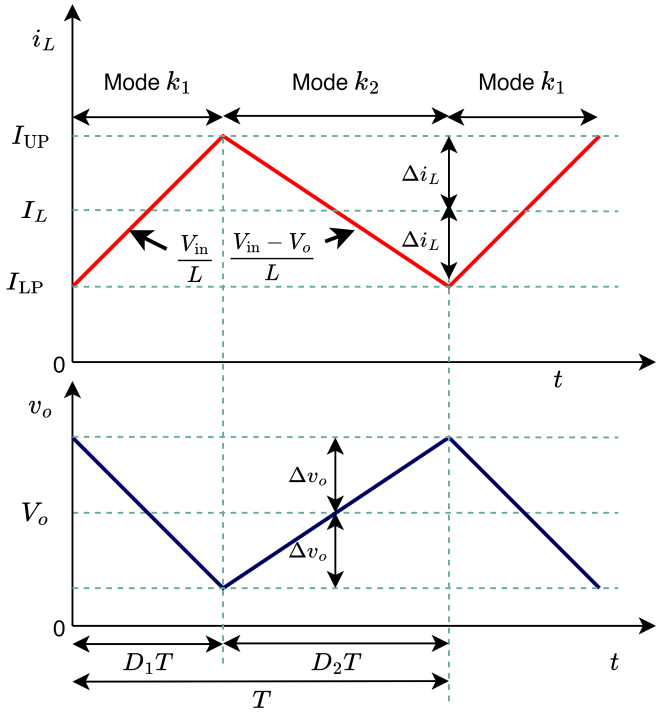



**Figure 3.4** Boost converter approximated waveforms of state variables in CCM

In a state of equilibrium, the average output voltage for the boost converter can be expressed as follows:

$$V_o = \frac{V_{in}}{1 - D_1} \tag{3.3}$$

During mode-$k_1$, the input voltage $V_{\mathrm{in}}$ appears across the inductor, resulting in a modification of the inductor current. The alteration in $i_L$ during this interval ($\Delta t = D_1 T$) can be represented as:

$$\frac{2\Delta i_L}{\Delta t} = \frac{V_{in}}{L} \tag{3.4}$$

By using (3.3) and (3.4), the ripple current is calculated as below:

$$\Delta i_L = \frac{V_{in}(V_o - V_{in})T}{2LV_o} \tag{3.5}$$

The average inductor current, $I_L$, can be obtained by equating the input and output power as shown below:

$$V_{in} \times I_L = V_o \times I_o \tag{3.6}$$

The inductor current $I_L$ is obtained from equation (3.6) in the following manner:

$$I_L = \frac{{V_o}^2}{RV_{in}} \tag{3.7}$$

Referring to Fig. 3.4, the peak inductor current during CCM operation can be represented as:

$$I_{UP} = I_L + \Delta i_L \tag{3.8}$$

From (3.8), the peak current of the inductor is influenced by both line and load conditions, and it is associated with the $J_{12} : i_L \geq I_{UP}$ which controls the shift from mode-$k_1$ to mode-$k_2$. Similarly, the transition from mode-$k_2$ to mode-$k_1$ is dictated by the $J_{21} : t \geq T$, where $T$ represents the time period.

**CCM/DCM detection Supervisor:** The design of the supervisor is essential to differentiate between CCM and DCM operations. In CCM operation, the inductor current is consistently greater than zero, while in DCM operation, it drops to zero momentarily. This change occurs when the ripple current of the inductor surpasses the average inductor current. Consequently, the distinct operating modes can be summarized as follows: $I_L > \Delta i_L \Rightarrow$ CCM operation, $I_L < \Delta i_L \Rightarrow$ DCM operation, and $I_L = \Delta i_L \Rightarrow$ Critical Conduction Mode (CrCM) operation.

### 3.3.2 PFM controller design for DCM

Under light load conditions, the inductor releases all its energy before the end of a switching cycle. This mode of operation is termed DCM. The graphical representation in Fig. 3.5 illustrates the estimated waveforms of the inductor current and output voltage during DCM operation.

Referring to Fig. 3.5, the value for the peak inductor current can be extracted as:

$$I_{UP} = slope \times time = \frac{V_{in}}{L} \times D_1 T \tag{3.9}$$

Applying the principle of volt-seconds balance, the average voltage across the inductor can be expressed as:

$$V_{in}D_1 + (V_o - V_{in})D_2 + (0)D_3 = 0 \tag{3.10}$$

The value of $D_2$ is determined using (3.10) in the following manner:

$$D_2 = \frac{D_1 V_o}{V_o - V_{in}} \tag{3.11}$$

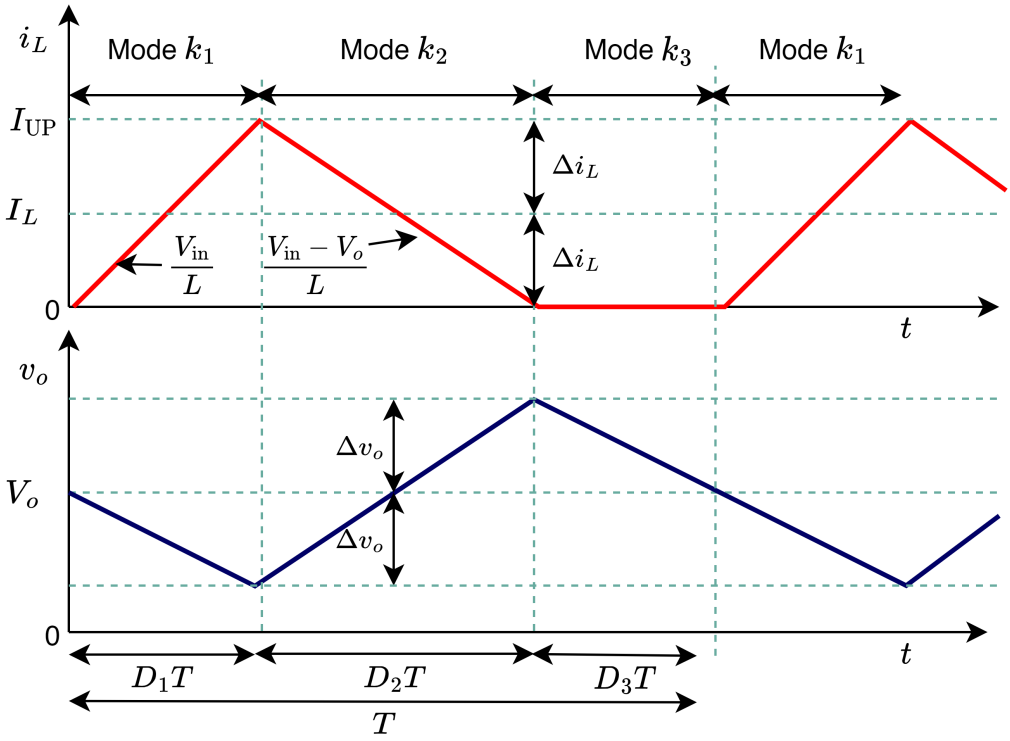



**Figure 3.5** Boost converter approximated waveforms of state variables in DCM

During the time interval $D_2T$, the average load current can be expressed as the current that flows through the diode. This can be mathematically represented as follows:

$$\frac{V_{in}D_1D_2}{2Lf} = \frac{V_o}{R} \tag{3.12}$$

The utilization of (3.11) and (3.12) leads to the derivation of a quadratic equation, which is presented as follows:

$$V_o^2 - V_oV_{in} - \frac{V_{in}^2D_1^2R}{2Lf} = 0 \tag{3.13}$$

The resolution of a quadratic equation (3.13) yields the following solution:

$$V_o = \frac{V_{in} \pm \sqrt{V_{in}^2 + \frac{4V_{in}^2D_1^2R}{2Lf}}}{2} \tag{3.14}$$

By rearranging the viable solution of (3.14), the expression for $D_1$ is derived as follows:

$$D_1 = \frac{1}{V_{in}}\sqrt{\frac{2V_o(V_o - V_{in})Lf}{R}} \tag{3.15}$$

By utilizing (3.9) and (3.15), the calculation for the peak inductor current during DCM

operation can be expressed as follows:

$$I_{UP} = \sqrt{\frac{2V_o(V_o - V_{in})}{RLf}} \tag{3.16}$$

According to (3.16), a low value of $f$ leads to an excessively high peak inductor current. Hence, selecting the right value for $f$ is crucial to avoid the adverse effects of high inductor current, including saturation, overheating, reduced efficiency, voltage spikes, electromagnetic interference, control issues, and noise generation in electronic circuits.

Thus, the peak current as per (3.16) determines the transition from mode-$k_1$ to mode-$k_2$. The transition from mode-$k_2$ to mode-$k_3$ is natural, and the output voltage swing is considered for the transition from mode-$k_3$ to mode-$k_1$. Thus, the $J$ for DCM operation are as follows: $J_{12}$:$i_L \geq I_{UP}$, $J_{23}$: $i_L = 0$, and $J_{31}$: $V_o \leq V_{ref}$.

## 3.4 Simulation Results and Analysis

The boundary-based hybrid control scheme proposed in this study is subjected to simulation through MATLAB/SIMULINK. The nominal parameters are configured as follows: $V_{\text{in}} = 15\,\text{V}$, $L = 100\,\mu\text{H}$, $C = 80\,\mu\text{F}$, $R = 20\,\Omega$, and $V_{\text{o}} = 30\,\text{V}$.

To achieve continuous transitions within SIMULINK, various components are employed to model and simulate the system's behavior. Conversely, when dealing with discrete transitions, a state flow chart is employed to depict the system's behavior. Stateflow, an extension of SIMULINK, enables users to model and simulate system behavior through a state machine. A state machine is a mathematical representation that characterizes a system's behavior as a collection of states and the transitions connecting them. The sequence of steps in the proposed approach is illustrated through the flow chart displayed in Fig. 3.6.

In order to assess the efficacy of the proposed approach, a comprehensive evaluation is performed by subjecting the system to a spectrum of line and load variations, depicted in Fig. 3.7. The collective results underscore the robustness and capability of the proposed control strategy in upholding stable operation across a spectrum of fluctuating conditions. The findings from this investigation, encapsulating key metrics such as duty cycle ($D$), percentage of peak overshoot ($\%M_p$), and settling time ($T_s$), across diverse scenarios of changes in line, load, and set-point, have been systematically organized in Table 3.3.

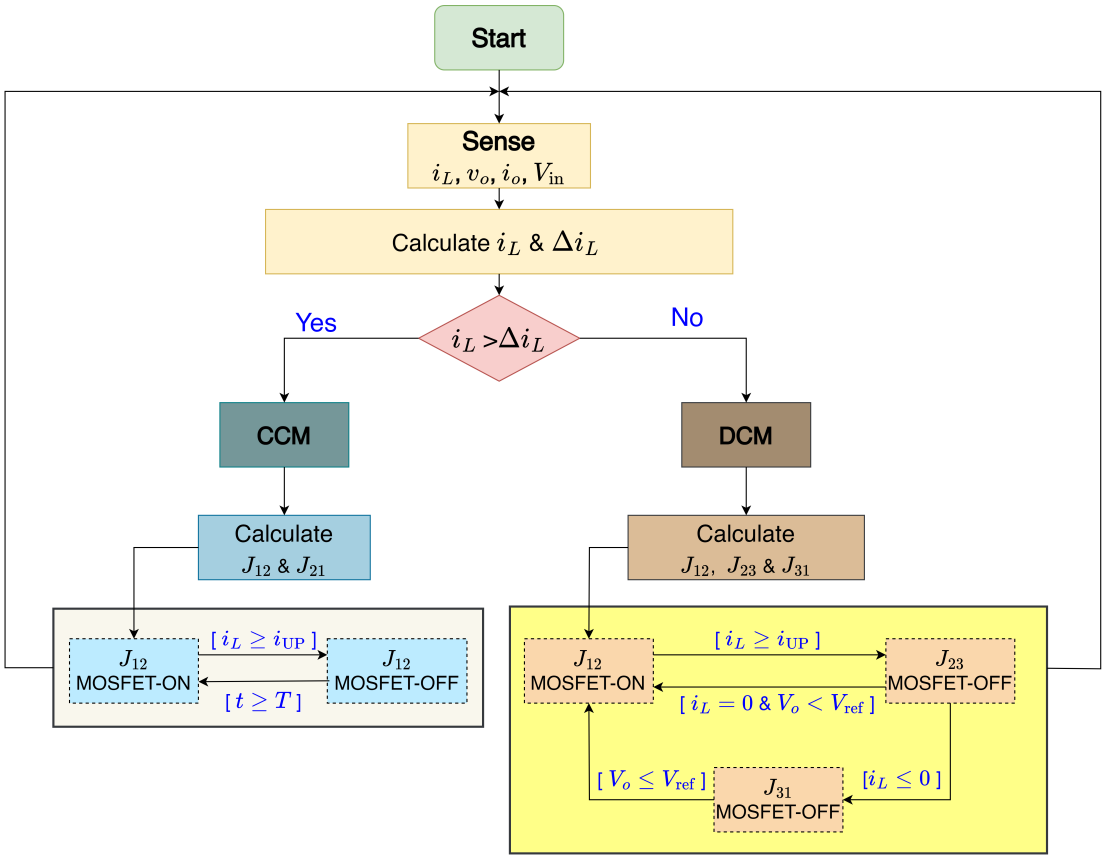



**Figure 3.6** Flow chart illustrating the boundary-based hybrid control algorithm for switched boost converter

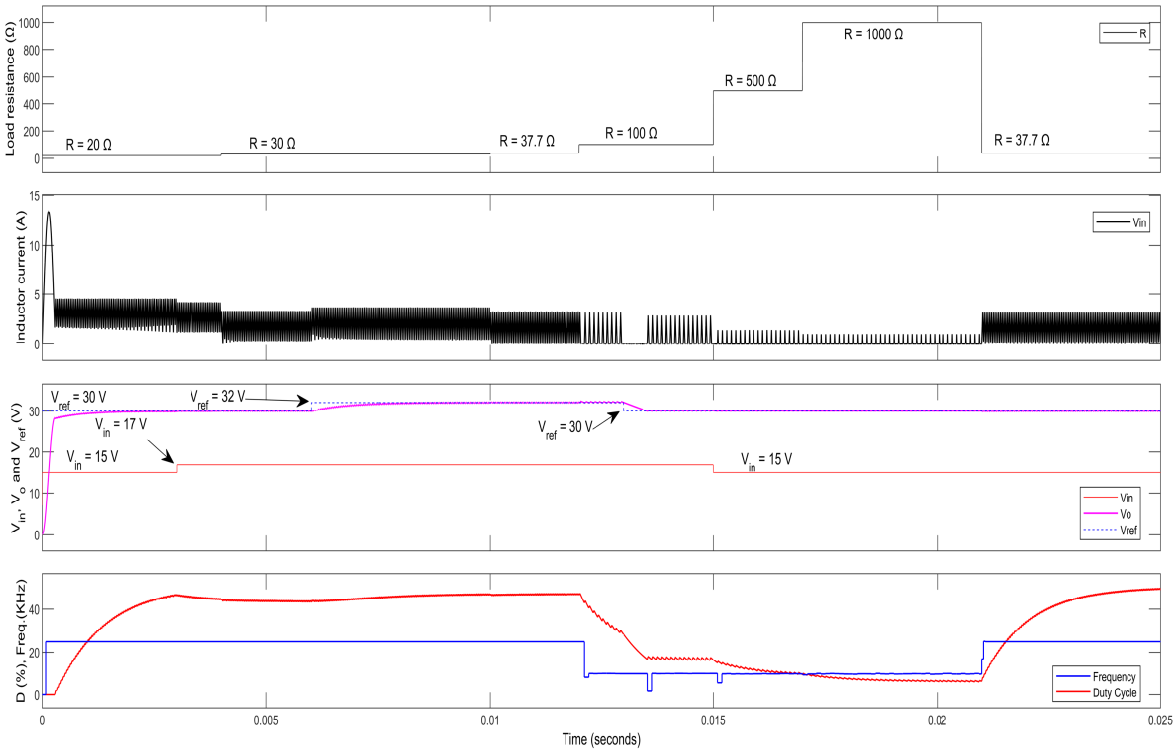



**Figure 3.7** Simulation outcomes for the boundary-based hybrid control applied to a boost converter, showcasing variations in **(a)** load resistance, **(b)** inductor current, **(c)** input voltage (red), reference voltage (blue), and output voltage (pink), and **(d)** frequency (blue), duty cycle (red)

**Table 3.3** $D$, $\%M_p$ , and $T_s$ analysis for boost converter under different scenarios

| Time span (ms) | $R$ (Ω) | $V_{in}$ (V) | $V_{ref}$ (V) | $D$ *(%)* | $\%M_p$ *(%)* | $T_s$ (ms) | Problem |
|---|---|---|---|---|---|---|---|
| [0-3) | 20 | 15 | 30 | [0-46.4) | 0 | 2.5 | - |
| [3-4) | 20 | 15 → 17 | 30 | [46.4-44.5) | 0 | 0 | Regulatory: Input voltage |
| [4-6) | 20 → 30 | 17 | 30 | [44.5-43.8) | 0.6 | 0.1 | Regulatory: Load |
| [6-10) | 30 | 17 | 30 → 32 | [43.8-46.9) | 0 | 3.5 | Servo: Set-point |
| [10-12) | 30 → 37.7 | 17 | 32 | [46.9-47.1) | 0.4 | 0 | Regulatory: Load |
| [12-13) | 37.7 → 100 | 17 | 32 | [47.1-28.8) | 1 | 0 | Regulatory: Load |
| [13-15) | 100 | 17 | 32 → 30 | [28.8-16.8) | 0 | 0.6 | Servo: Set-point |
| [15-17) | 100 → 500 | 17 → 15 | 30 | [16.8-9.7) | 0 | 0 | Regulatory: Input voltage + Load |
| [17-21) | 500 → 1000 | 15 | 30 | [9.7-6.5) | 0 | 0 | Regulatory: Load |
| [21-25) | 1000 → 37.7 | 15 | 30 | [6.5-48.9) | 0.6 | 1 | Regulatory: Load |

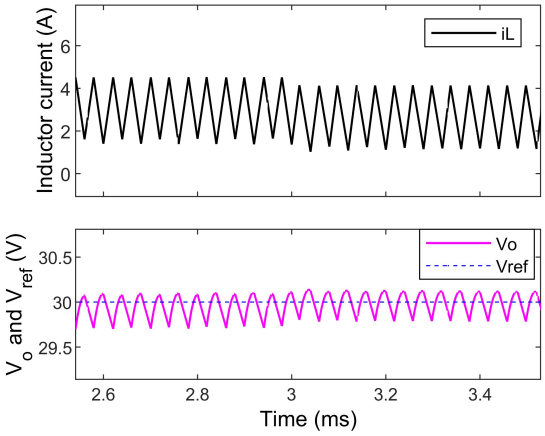
In the subsequent subsections, a thorough analysis of the simulation results is presented, aiming to provide a profound understanding of the observed trends, implications, and performance under various conditions.

### 3.4.1 CCM operation

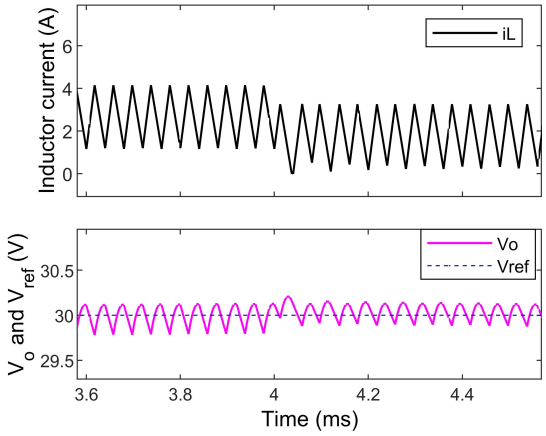
The simulation begins at $t$ = 0 with initial conditions: $V_{in}$ = 15 V, $R$ = 20 Ω, $V_{ref}$ = 30 V, and $f$ = 25 kHz. Upon activation, the alignment of the output voltage of the switched boost converter with the set-point is promptly achieved, showcasing a swift response without any overshoot. Hereafter, the disturbances and outcomes are consolidated as follows.

- **Line voltage variation:** At $t$ = 3 ms, the line voltage changes from $V_{in}$ = 15 V to 17 V. As depicted in Fig. 3.8a, the corresponding waveforms of $i_L$ and $v_o$ reveal an absence of overshoot in the output voltage waveform.
- **Load variation:** A load variation is introduced at $t$ = 4 ms, with the $R$ transitioning from 20 Ω to 30 Ω. Fig. 3.8b illustrates the $i_L$ and $v_o$ waveforms associated with this change. It's noteworthy that the output voltage rapidly converges to the desired value with minimal overshoot.
- **Set-Point change:** To evaluate the voltage tracking capability of the controller under CCM operation, a set-point change from $V_{ref}$ = 30 V to 32 V is initiated at $t$ = 6 ms. The variations in state variables are shown in Fig. 3.8c, clearly indicating that the output voltage reaches the new set-point within 3 ms.

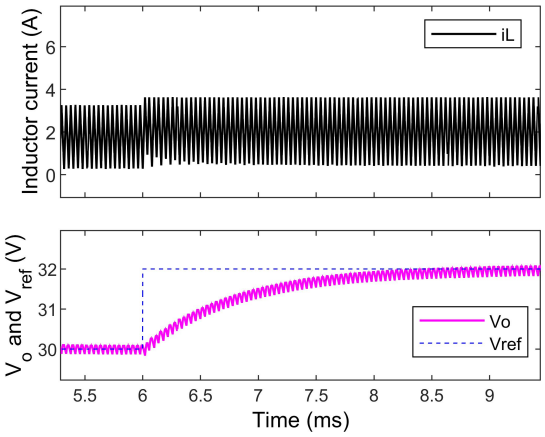
- An abrupt decrease in load is introduced, where the $R$ is lowered from 1000 Ω to 37.7 Ω at $t$ = 21 ms. This is done to assess the performance of the control scheme during the transition from DCM to CCM operation. Remarkably, the output voltage remains well-regulated even in this challenging scenario, as depicted in Fig. 3.8d.



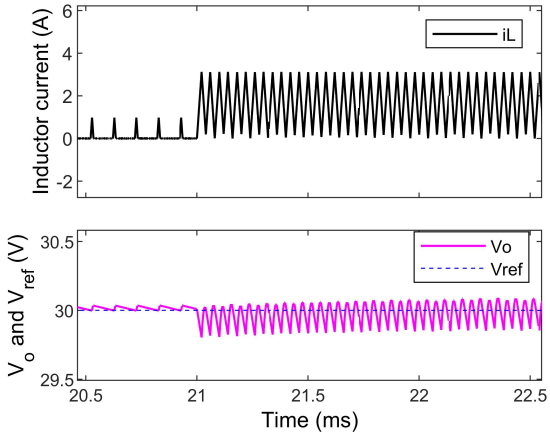

**(a)** Step-up change in $V_{in}$ from 15 V to 17 V at $t$ = 3 ms




**(b)** Step-up change in $R$ from 20 Ω to 30 Ω at $t$ = 4 ms




**(c)** Step-up change in $V_{ref}$ from 30 V to 32 V at $t$ = 6 ms




**(d)** Step-down change in $R$ from 1000 Ω to 37.7 Ω at $t$ = 21 ms

**Figure 3.8** State-variables behavior of boost converter with the proposed scheme in CCM

### 3.4.2 CrCM operation

In the context of line and load fluctuations, a distinctive operational state arises, characterized by a brief interruption in inductor current followed by a rapid recovery. This intriguing behavior is coined as CrCM, which is also recognized as boundary conduction mode [87]. The manifestation of this mode in power converters represents a critical boundary between CCM and DCM. Fig. 3.9 provides insight into this phenomenon by showcasing state variable waveforms during a distinctive event: a step change in load. Specifically, the $R$ undergoes a

transition from 30 Ω to 37.7 Ω at $t$ = 10 ms. What is remarkable in this display is the subtle variation in the $v_o$, accompanied by an almost negligible steady-state error. The system not only maintains stability during this transition but also demonstrates a remarkable ability to trace the reference voltage without encountering significant challenges.

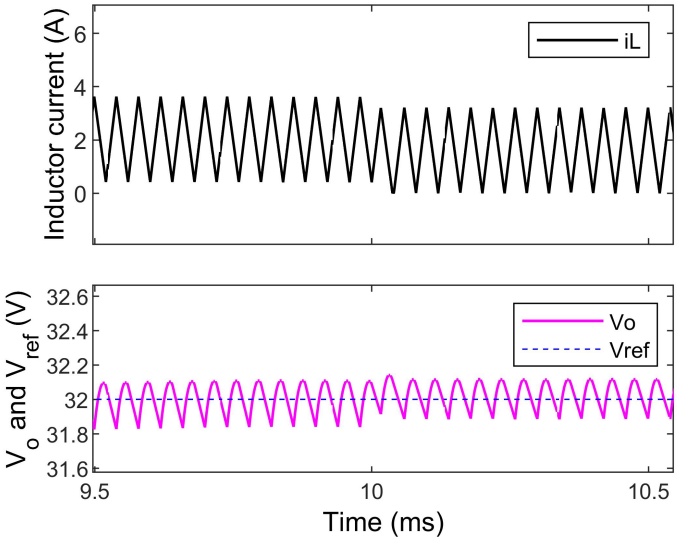



**Figure 3.9** State-variables behavior of boost converter with the proposed scheme to a load change from 30 Ω to 37.7 Ω at $t$ = 10 ms resulting in CrCM operation

### 3.4.3 DCM operation

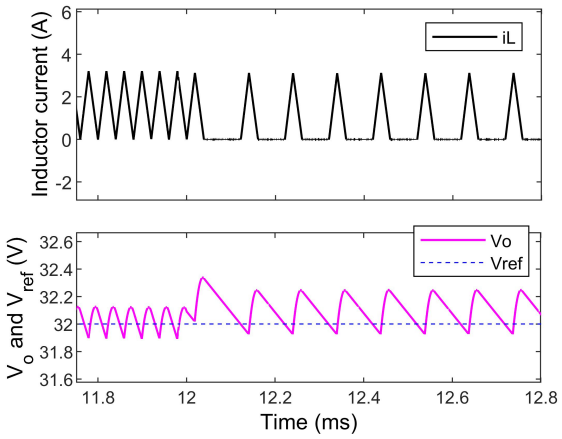
To mitigate losses during DCM operation, $f$ = 10 kHz is chosen. Disturbances encountered in DCM operation are outlined below.

- At $t$ = 12 ms, an abrupt increase in the load resistance to $R$ = 100 Ω from 37.7 Ω results in seamless DCM operation. Fig. 3.10a displays the corresponding waveforms of $i_L$ and $v_o$. Thus, even when transitioning from CCM to DCM, the controller adeptly follows $V_{ref}$ and demonstrates stability.

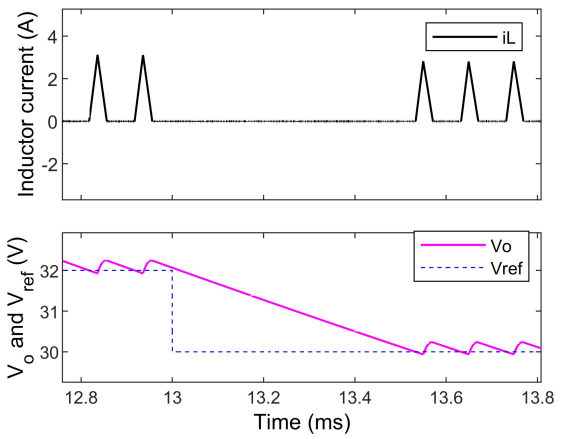
- Introducing a negative set-point change from $V_{ref}$ = 32 V to 30 V at $t$ = 13 ms evaluates the voltage tracking capabilities of the controller in DCM operation. Fig. 3.10b depicts nearly 1 ms of the absent inductor current, where the capacitor energizes the load. Absence of inductor current occurs as the output voltage exceeds the reference voltage, resulting in the MOSFET turning OFF, while the diode prevents current back-flow.

- To further probe the controller's robustness, concurrent line and load changes are examined. At $t$ = 15 ms, while augmenting the load from $R$ = 100 Ω to 500 Ω, the input voltage drops from $V_{in}$ = 17 V to 15 V. Impressively, the output maintains stability without exhibiting over or undershoot, as depicted in Fig. 3.10c.

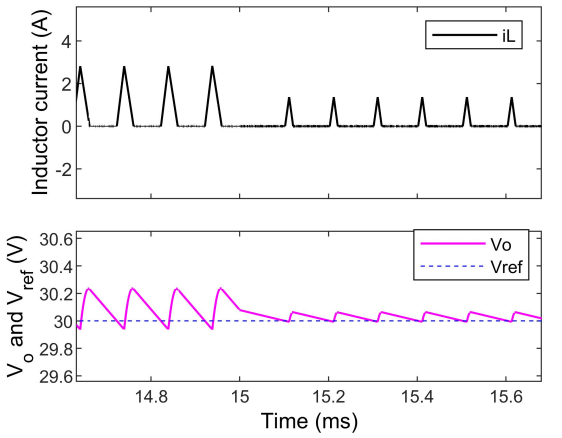
- Subsequently, increasing the load to $R$ = 1000 Ω from 500 Ω at $t$ = 17 ms showcases the controller's adeptness in tracking the output voltage, as showcased in Fig. 3.10d.



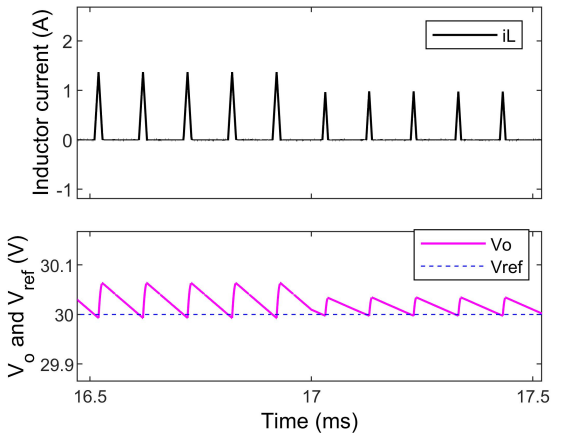

**(a)** Step-up change in $R$ from 37.7 Ω to 100 Ω at $t$ = 12 ms




**(b)** Step-down change in $V_{ref}$ from 32 V to 30 V at $t$ = 13 ms




**(c)** Step-up change in $R$ from 100 Ω to 500 Ω and a step-down change in $V_{in}$ from 17 V to 15 V at $t$ = 15 ms




**(d)** Step-up change in $R$ from 500 Ω to 1000 Ω at $t$ = 17 ms

**Figure 3.10** State-variables behavior of boost converter with the proposed scheme in DCM

### 3.4.4 Parametric variations analysis

While a significant number of servo and regulatory issues have been addressed, and the controller's stability has been established in the face of various disturbances, it's essential to acknowledge the possibility of variations in component parameters, particularly those associated with the inductor and capacitor. Therefore, a comprehensive examination is conducted to evaluate the possible consequences arising from parameter variations associated with these two components. This examination allows for a more comprehensive understanding of how parameter fluctuations might influence the system's behavior.

**Inductor variations:** A variation of ±20% in the inductor is taken into account. The inductor, a key component in the boost converter, can exhibit such variations due to manufacturing tolerances, temperature fluctuations, and material properties. These factors can lead to discrepancies in the inductance value, which in turn affect the converter's behavior, such as output voltage regulation, transient responses, and stability. Incorporating these inductor variations in the analysis allows for a comprehensive evaluation of the proposed control scheme's effectiveness under different conditions.

When the inductance is reduced by 20%, the output voltage of the boost converter remains relatively unaffected, mainly due to faster current buildup during the switching cycle's on-time. This compensates for the reduced inductance's impact on energy storage. However, this reduction in inductance leads to an increase in inductor ripple current, which is managed by the proposed controller to maintain output voltage stability. Conversely, when the inductance is increased by 20%, the output voltage gradually decreases due to slower current buildup during the on-time. This is accompanied by a decrease in inductor ripple current, as the larger inductance requires lower current fluctuations. These variations are illustrated in Fig. 3.11, showcasing the effectiveness of the proposed controller in handling inductance variations while ensuring stable output voltage regulation.

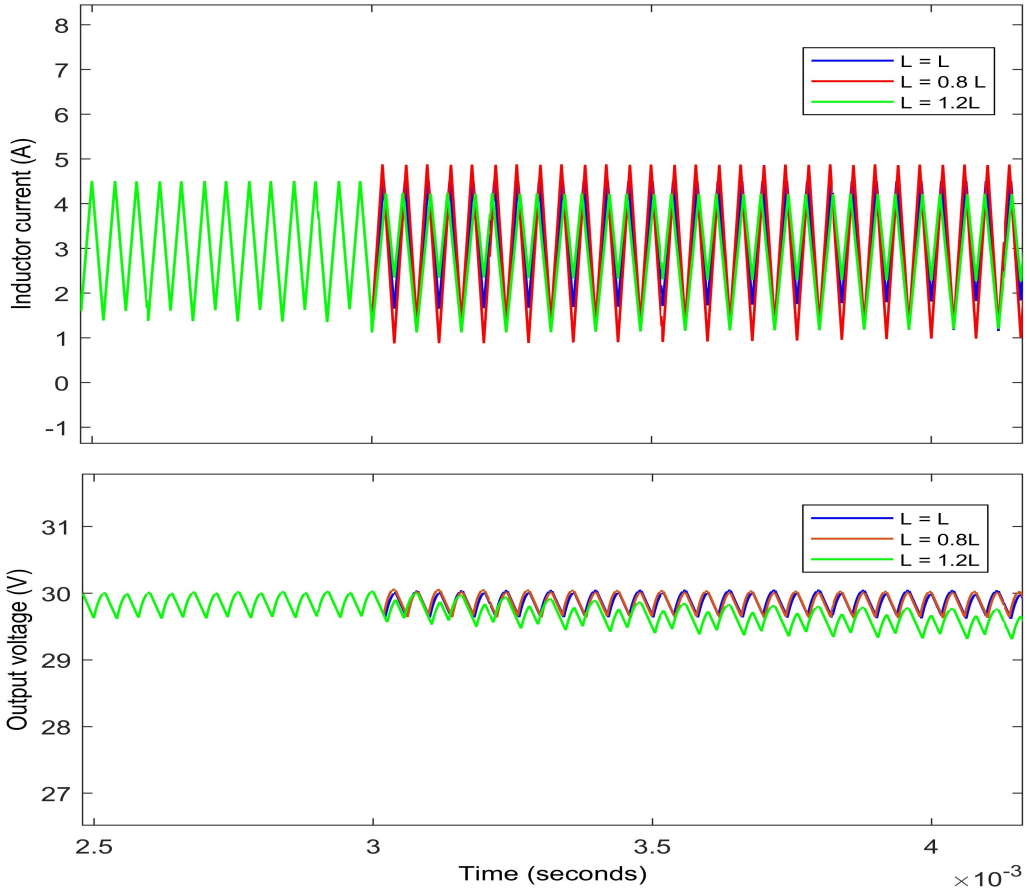



**Figure 3.11** Analysis of boost converter with the proposed scheme under ±20% inductance variations

**Capacitor variations:** The consideration of ±20% variations in the capacitor value introduces potential changes in the behavior of the boost converter. These variations can arise from manufacturing tolerances, ageing effects, temperature fluctuations, or changes in the dielectric properties of the capacitor material. Such factors can lead to differences in capacitance values from their nominal specifications, influencing the energy storage and discharge characteristics of the capacitor during the switching cycles. These variations can result in shifts in the voltage and current waveforms across the converter's components, potentially impacting the overall performance and stability of the system. Hence, it is essential to assess these variations when evaluating the proposed controller's effectiveness.

A reduction of 20% in the capacitor value leads to a slight increase in the output voltage ripple, primarily due to the reduced energy storage capacity of the capacitor. On the other hand, a 20% increase in capacitance causes a sudden drop in the output voltage, followed by a gradual settling to the desired value. This behavior is attributed to the increased energy storage capacity of the capacitor, resulting in slower voltage discharge during the switching cycle. Additionally, the increased capacitance contributes to a reduction in inductor current ripple. The proposed controller effectively mitigates these variations, maintaining output voltage stability and regulating inductor current. These responses to capacitance variations are demonstrated in Fig. 3.12.

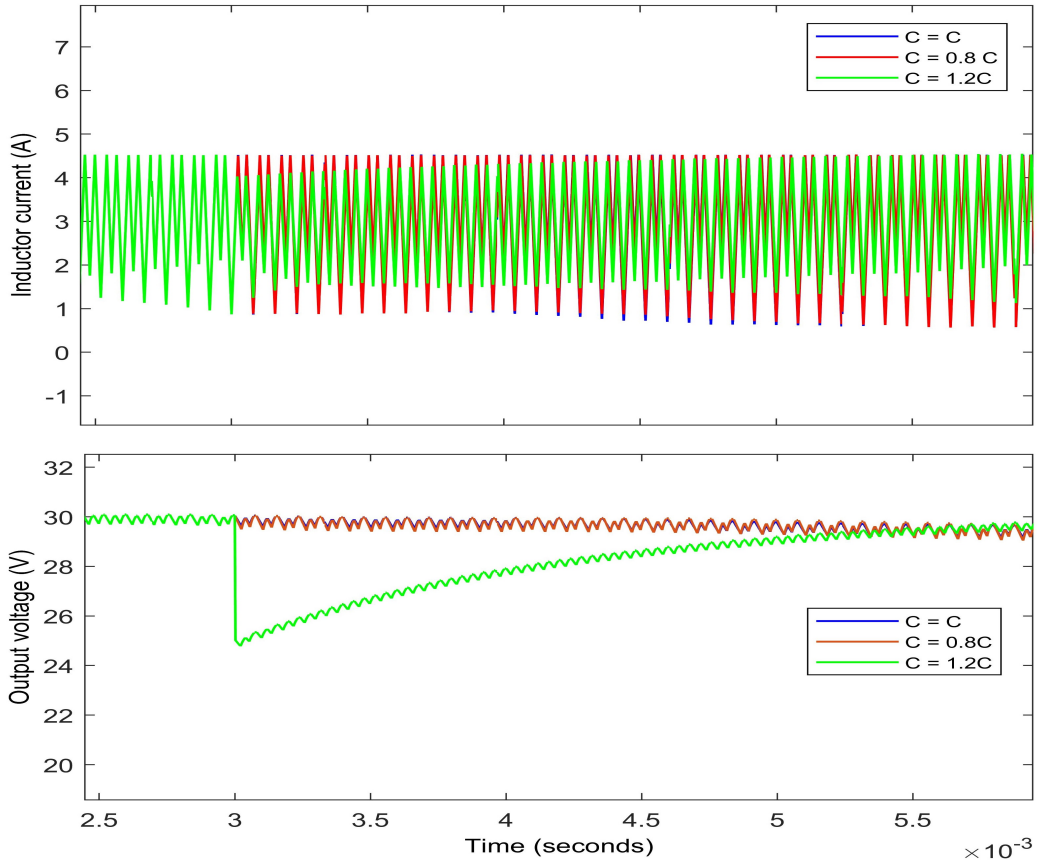



**Figure 3.12** Analysis of boost converter with the proposed scheme under ±20% capacitance variations

## 3.5 Comparative Analysis

A comparative study is crucial as it allows for a thorough assessment of different approaches. This analysis helps in understanding their individual strengths and limitations within a unified context. Such an examination aids in making informed decisions to optimize solutions based on specific requirements.

### 3.5.1 Comparative analysis with conventional control schemes

Table 3.4 presents a comprehensive comparison among the proposed control scheme, the PID control scheme, and the FOPID control scheme. This comparison aims to clarify the unique characteristics and potential advantages inherent in the proposed scheme. By comparing these control approaches, a deeper understanding of their comparative strengths and weaknesses can be gained.

The design parameters employed for this analysis are as follows: $V_{in}$ = 5 V, $L$ = 150 $\mu$H, $C$ = 200 $\mu$F, $R$ = 30 Ω, $f$ = 5000 Hz, and a $V_{ref}$ of 12 V [34]. Employing the proposed method, the obtained outcomes stand out due to their complete absence of any overshoot or undershoot behaviors. While it is worth noting that a slightly higher ripple is observed when compared to the FOPID control strategy, the proposed method showcases a remarkable enhancement in both rise time and slew rate characteristics. These notable enhancements in transient behavior indicate its ability to respond quickly to changes and sustain stable operation. In Fig. 3.13, a comprehensive representation of the resulting output voltage variations is depicted, providing a visual insight into the system's performance under this approach.

**Table 3.4** Boost converter comparative performance evaluation: PID vs. FOPID vs. Proposed Scheme

| Parameter | PID [34] | FOPID [34] | Proposed scheme |
|---|---|---|---|
| $V_o$ (V) | 11.61 | 11.99 | **12** |
| Rise time ($\mu$s) | 432.533 | 606.711 | **269.770** |
| Slew rate (mV/ms) | 21.839 | 15.805 | **26.362** (V/ms) |
| $\Delta v_o$ (V) | 0.5 | **0.001** | 0.125 |
| $\%M_p$ (%) | 27.564 | 1.531 | **0** |
| Undershoot (%) | -1.047 | 1.032 | **0** |
| $T_s$ (ms) | 19.919 | **0.432** | 3 |

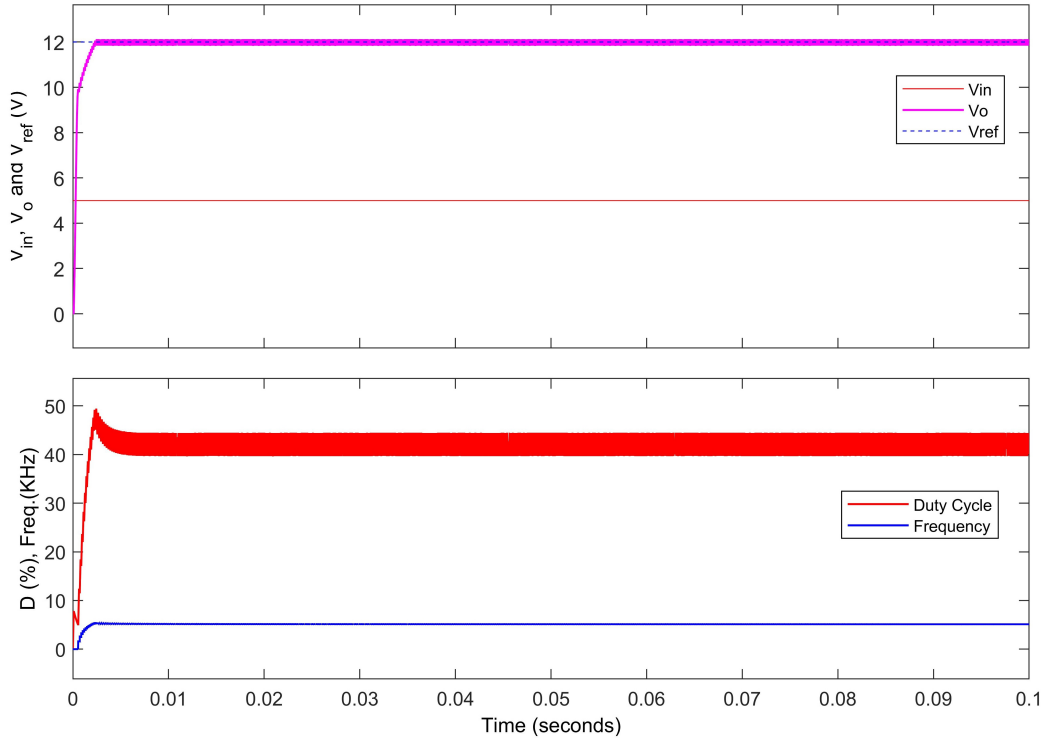



**Figure 3.13** Boost converter waveforms with proposed scheme for comparative analysis with PID and FOPID

### 3.5.2 Comparative analysis with state-of-the-art techniques

The comparison of the proposed scheme extends to encompass a range of ADRC techniques. These techniques include Generalized ADRC (GADRC), Modified ADRC (MADRC), Linear ADRC (LADRC), Higher Control Gain ADRC (HADRC), Filtered Derivative Feedback Control ADRC (NADRC), and GPI Observer-based ADRC (GPI-ADRC) [43]. The focal point of this comparison lies in evaluating the performance of the proposed scheme against these ADRC variants. Notably, the considered nominal parameters are as follows: $V_{in}$= 30 V, $L$ = 500 $\mu$H, $C$= 1000 $\mu$F, $R$ = 50 Ω, $f$ = 15000 Hz, and $V_{ref}$ = 50 V.

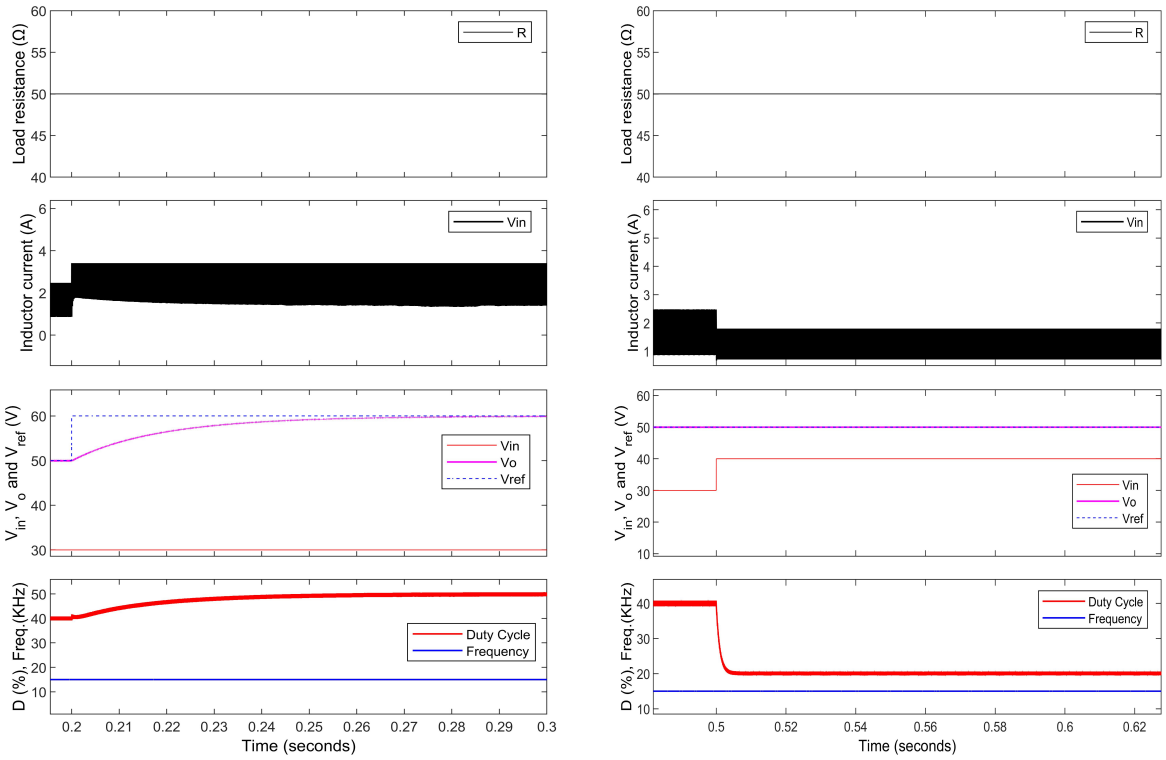
In the first scenario (Case-1), a transition is observed where $V_{ref}$ shifts from 50V to 60V at $t$ = 0.2 seconds. Conversely, in the second scenario (Case-2), a change in $V_{in}$ occurs, moving from 30 V to 40 V at $t$ = 0.5 seconds. On evaluating the system responses, the proposed scheme demonstrates a slightly slower response in tracking the set-point change for Case-1. Nevertheless, it stands out with improvements in minimizing overshoot and restricting maximum inductor current.

Significantly, exceptional outcomes are revealed in Case-2. The proposed scheme showcases robustness, leading to minimal disturbance in the output voltage, absence of noticeable overshoot, and notably restrained inductor current variations. This performance highlights the scheme's agility in rapidly adapting to input voltage changes.

The comprehensive comparative analysis for both cases is detailed in Table 3.5. Furthermore, Fig. 3.14a and Fig. 3.14b clearly show the waveforms for Case-1 and Case-2, giving a visual idea of how the scheme behaves in different situations.

**Table 3.5** Boost converter control performance: proposed scheme vs. ADRC approaches

| Problem | Case-1 (Servo) [43] | | | Case-2 (Regulatory: Input Voltage) [43] | | |
|---|---|---|---|---|---|---|
| Algorithm | $T_s$ (ms) | $M_p$ (V) | $I_{L(MAX)}$ (A) | $T_s$ (ms) | $M_p$ (V) | $I_{L(MAX)}$ (A) |
| LADRC | 18.3 | 4.88 | 4.88 | 23.1 | 3.1 | 2.90 |
| HADRC | 22.0 | 5.17 | 5.17 | 29.0 | 4.6 | 3.87 |
| NADRC | 12.4 | 5.79 | 5.79 | 17.3 | 4.0 | 3.22 |
| GADRC | 12.8 | 5.81 | 5.81 | 17.2 | 4.1 | 3.25 |
| GPI-ADRC | 16.1 | 5.18 | 5.18 | 18.1 | 1.5 | 2.89 |
| MADRC | **12.0** | 5.82 | 5.82 | 16.4 | 3.5 | 3.00 |
| Proposed | 35.0 | **0.00** | **3.40** | **0.00** | **0.0** | **1.80** |




**(a)** Simulation outcome: Proposed scheme in case-1 **(b)** Simulation outcome: Proposed scheme in case-2

**Figure 3.14** Boost converter waveforms with proposed scheme for comparative analysis with ADRC techniques

## 3.6 Summary

In this extensive study, the boost converter's foundational theory and core principles are introduced. Its modeling is examined, utilizing both state-space and hybrid automaton approaches. Subsequently, a boundary-based hybrid controller is created using PWM for CCM operation and PFM for DCM operation. Rigorous simulations cover various scenarios, demonstrating the efficacy of the scheme. Robustness is validated against component variations. Lastly, a comparison is made between proposed approach and PID, FOPID, and ADRC techniques, showcasing the superiority of the proposed control scheme. The excel of proposed control scheme in boost converter applications is established by this comprehensive exploration.

# CHAPTER-4

# Control of DC-DC Buck Converter

In this chapter, the intricacies of buck converter control are examined to make its fundamental principles and strategies easier to understand. Additionally, a simplified modeling approach is introduced, using SDS and hybrid automaton techniques. This approach has proven highly effective in accurately depicting how the buck converter behaves under various conditions.

A key point in this study is the detailed simulation results and useful comparisons. These results help connect the theoretical ideas to real-world use, making it easier to understand how buck converter control works. This improved understanding not only strengthens the theory behind this technology but also has important implications for its reliability in real-life situations.

## 4.1 Fundamental Insights into Buck Converter Operation

A buck converter is a type of DC-DC power converter designed to reduce the output voltage from a DC source. Fundamentally, it utilizes key components such as an inductor, a switching element (usually a transistor), a diode, and a capacitor. These elements work in synergy to achieve the desired voltage reduction, as depicted in Fig. 4.1 [83]. While the analysis assumes ideal components, the compensation mechanism addresses the parametric variations and parasitic values.
The fundamental operation of the buck converter can be described as follows:

- **Inductor charging (On-state):** When the transistor is turned on, current flows from the input source through the inductor and the load (output) resistor. The inductor resists changes in current, causing it to store energy in the form of a magnetic field.
- **Inductor discharging (Off-state):** When the transistor is turned off, the current path through the inductor is interrupted. The inductor's stored energy seeks to maintain current flow, causing it to discharge into the load.

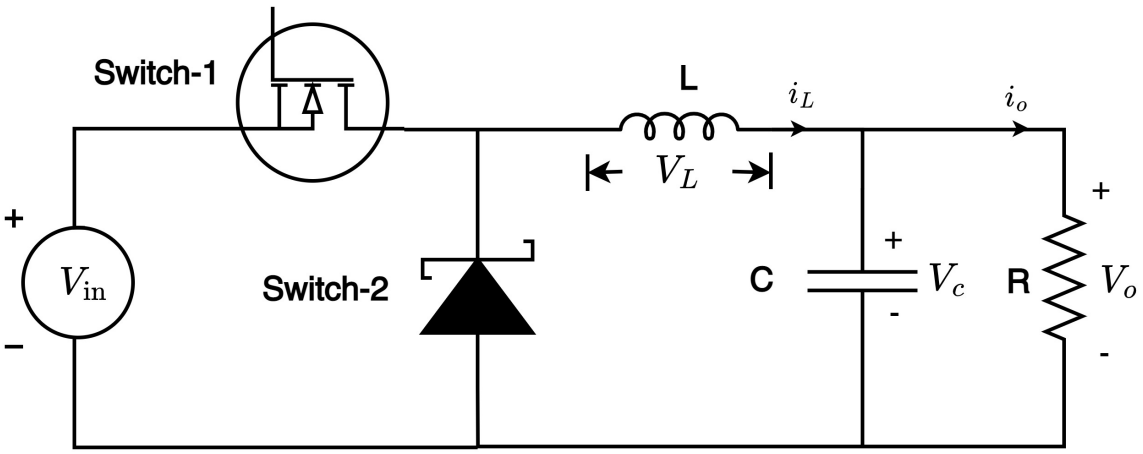



**Figure 4.1** Typical switched buck converter circuit diagram

- **Diode action:** During the transistor's off state, a diode provides a path for the inductor's current to continue flowing, sustaining the energy transfer to the load.
- **Output capacitor usage:** An output capacitor is connected in parallel to the load to smooth out voltage ripples caused by the switching action. It stores energy during high-output periods and releases it during low-output periods.
- **Regulation:** To maintain a stable output voltage, a feedback loop compares the actual output voltage with a reference voltage. The controller adjusts the duty cycle of the switching element based on the feedback, ensuring that any changes in the load or input voltage are compensated for.

## 4.2 Modeling of Buck Converter

The primary objective involves developing a precise representation of the buck converter's behavior within the context of SDS. This task involves constructing mathematical equations that describe the correlations among critical variables, including input voltage, output voltage, inductor current, and switch states. By leveraging the principles of SDS, the modeling procedure aims to capture the dynamic variations that arise during switching transitions, offering insights into both the transient and steady-state characteristics of the converter. Through this thorough analysis, a better understanding of how the buck converter operates is achieved. This sets the foundation for developing more advanced control methods within the SDS framework.

### 4.2.1 State-space modeling of buck converter

The modeling approach used for the buck converter mirrors that employed for the boost converter in (3.1). However, for the sake of simplicity, it is restated below:

$$\dot{x}(t) = A_k x(t) + B_k \tag{4.1}$$

Where $x \in X$ is state vector, $A_k \in R^{n \times n}$ is system matrix and $B_k \in R^{n \times 1}$.

Since the buck converter also integrates two switches, this configuration leads to the emergence of four discrete states. The corresponding state matrices for these states are presented in Table 4.1, while the circuits for each state are shown in Fig. 4.2. Significantly, the discrete state $k_3$ is linked with DCM, while $k_4$ is deemed unfeasible. For buck converter controller design, the focus is solely on CCM.

**Table 4.1** Buck converter possible discrete state and corresponding system state matrices

| Operating mode ($K_i$) | Switch-1 | Switch-2 | $A_i$ | $B_i$ |
|---|---|---|---|---|
| $k_1$ | ON | OFF | $\begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}$ | $\begin{bmatrix} \frac{V_{in}}{L} \\ 0 \end{bmatrix}$ |
| $k_2$ | OFF | ON | $\begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}$ | $\begin{bmatrix} 0 \\ 0 \end{bmatrix}$ |
| $k_3$ | OFF | OFF | $\begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix}$ | $\begin{bmatrix} 0 \\ 0 \end{bmatrix}$ |
| $k_4$ | ON | ON | Impractical | |

### 4.2.2 Hybrid automaton representation of buck converter

The modeling of the buck converter follows a similar approach as the boost converter, employing the same mathematical equation (3.2) for analysis, as illustrated below.

$$\dot{x}(t) = f_\sigma(x(t)) \tag{4.2}$$

Where $x(t)$ is the state of the system at time $t$, $\dot{x}(t) = f_\sigma(x(t))$ is the state-transition function, which describes the dynamics of the system in the $\sigma$ mode of operation. The operation of

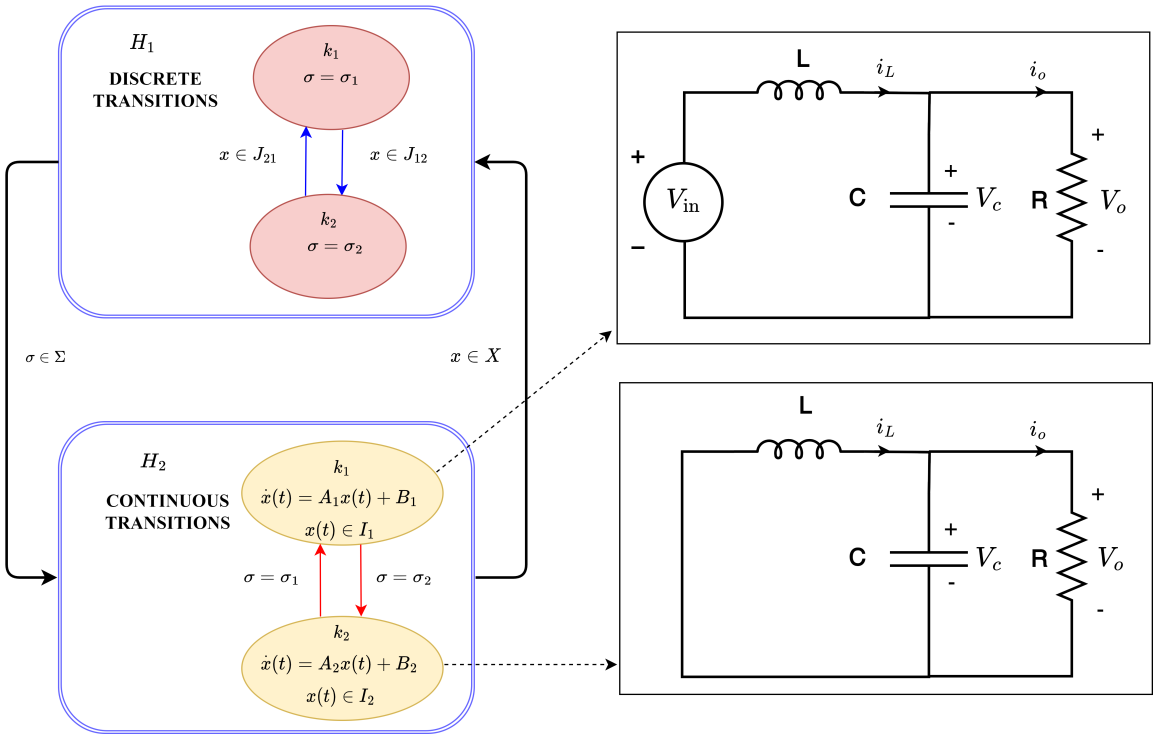



**Figure 4.2** Hybrid automaton representation of DC-DC buck converter for CCM: Interplay between continuous and discrete transitions with mode circuits

the system is determined by a switching signal $\sigma$ that is defined by a set of state-dependent boundaries.

The buck converter is conceptualized as an SDS that operates in two distinct modes:

1. When the MOSFET is in the ON state, the system's behavior is characterized by a Linear Time-Invariant (LTI) model. In this mode, the input voltage is applied to the inductor, and the output voltage is controlled through the diode's switching operation.

2. Conversely, when the MOSFET switches to the OFF state, the system enters a different LTI mode. During this phase, the inductor discharges into the output capacitor, leading to a noticeable decrease in voltage.

The buck converter, consisting of passive components and switches, showcases a blend of continuous and discrete behaviors. This hybrid nature is effectively demonstrated using the accompanying hybrid automaton, as illustrated in Fig. 4.2. This concept is encapsulated by the tuple $\mathcal{H} = \{K, X, F, I, E, g, J\}$, encompassing key elements that define its operation and dynamics. This closely aligns with the composition of a boost converter as discussed in section 3.2.2.

## 4.3 Development of Buck Converter Control Strategy

Within the framework of the SDS model, the challenge of controlling a buck converter can be streamlined by focusing on the choice of $J$, which establishes the foundation for a consistent frequency PWM strategy. In the realm of closed-loop control, the buck converter's continuous and discrete transitions are governed by specific boundary conditions dictated by the $J$. The continuous transitions are regulated by boundary conditions determined by the inductor current and output voltage, whereas discrete transitions are orchestrated through the activation and deactivation of the MOSFET. Whenever the continuous-time variable surpasses the predefined limits set by $J$, it triggers the initiation of discrete transitions. In the CCM operation of a buck converter as shown in 4.2, the transition points between the continuous and discrete modes, denoted as $J_{12}$ and $J_{21}$, are collectively referred to as $J$.

Fig. 4.3 illustrates approximated waveforms for the inductor current and output voltage of the buck converter operating in CCM.

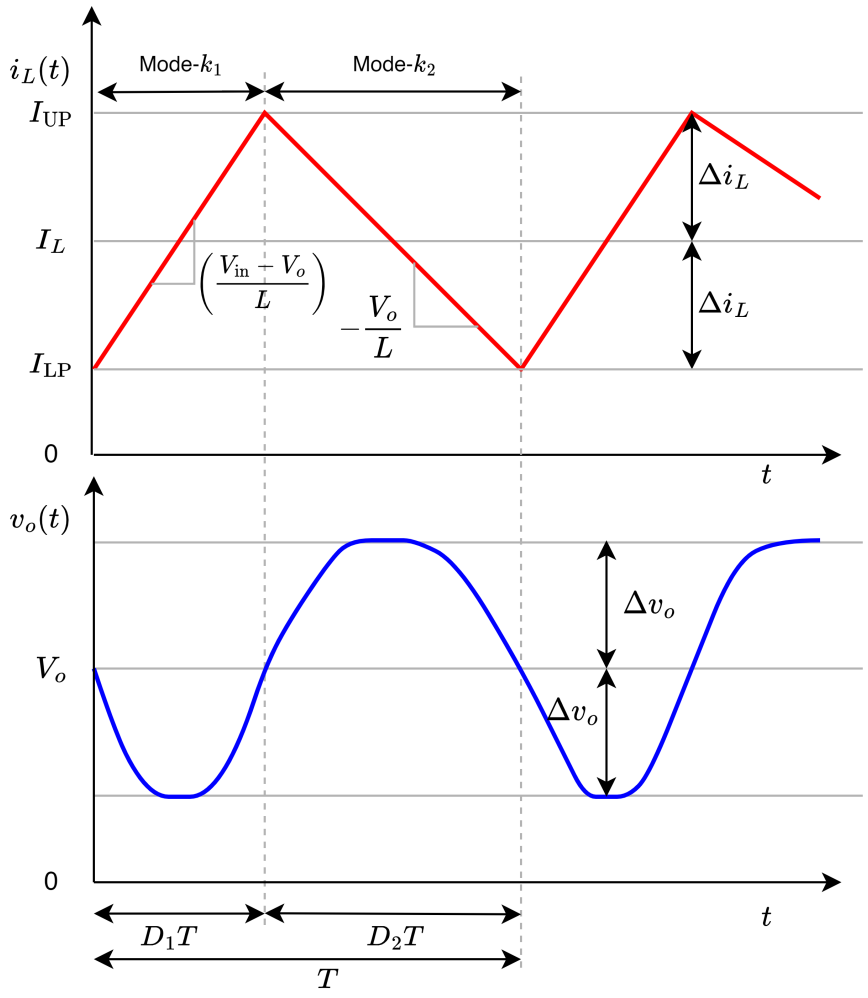



**Figure 4.3** Buck converter approximated waveforms of state variables in CCM

The calculation for the voltage across the inductor while the MOSFET is in the ON state is as follows:

$$V_{L(ON)} = -(V_{in} - V_o) \tag{4.3}$$

The calculation for the inductor voltage during the OFF state of the MOSFET can be determined as follows:

$$V_{L(OFF)} = V_o \tag{4.4}$$

In a steady-state condition, the average inductor current within one cycle equates to zero, which can be expressed as follows:

$$V_{L(ON)} D_1 T + V_{L(OFF)} D_2 T = 0 \tag{4.5}$$

Expressing $D_2T$ as $(T - D_1T)$ and substituting Equation (4.3) and (4.4) into (4.5) while solving for $D_1$ yields the following result:

$$D_1 = \frac{V_o}{V_{in}} \tag{4.6}$$

Calculation of the change in inductor current can be performed as follows:

$$2\Delta i_L = I_{UP} - I_{LP} = \frac{V_{in} - V_o}{L} D_1 T \tag{4.7}$$

Upon substituting (4.6) into (4.7), the following expression is obtained:

$$\Delta i_L = \frac{V_o (V_{in} - V_o) T}{2 L V_{in}} \tag{4.8}$$

The average inductor current for a buck converter operating in CCM is given by:

$$I_L = \frac{V_o}{R} \tag{4.9}$$

Ultimately, $J_{12}$ is defined as follows:

$$J_{12} : i_L \geq I_{UP} \implies I_L + \Delta i_L \tag{4.10}$$

Likewise, $J_{21}$ can be expressed as:

$$J_{21} : t \geq T \tag{4.11}$$

Fig. 4.4 presents the block diagram of the closed-loop control scheme, which includes integral compensation to address parasitic values. A more comprehensive examination of the integral compensation technique is elaborated upon in the next section.

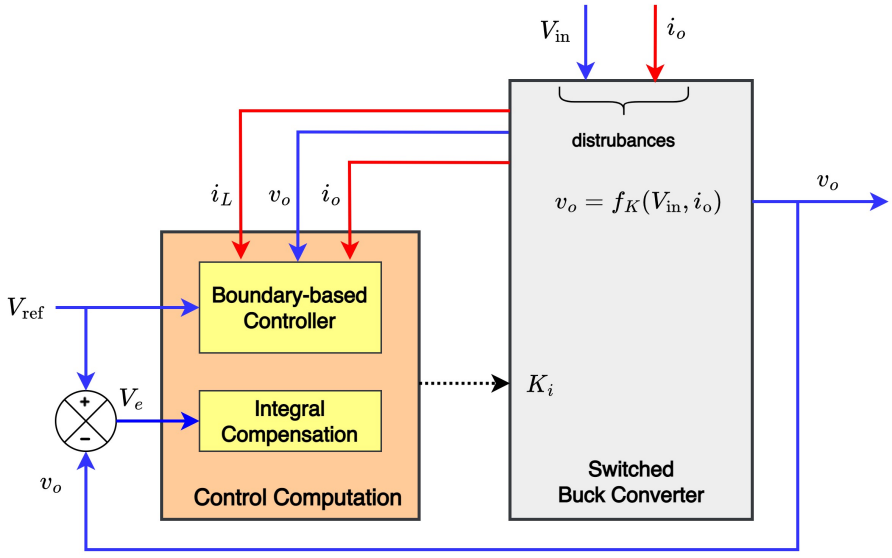



**Figure 4.4** The proposed closed-loop control scheme for buck converter

## 4.4 Simulation Results and Analysis

The proposed control scheme underwent a thorough evaluation through simulation utilizing MATLAB/SIMULINK. The simulation was conducted with nominal parameters for the buck converter, as outlined in Table 4.2. The simulation framework was structured with a diagram, visually represented in Fig. 4.5, which demonstrated the interconnected components within MATLAB/SIMULINK. The outcomes of the simulation are vividly illustrated in Fig. 4.6, showcasing the performance and behavior of the control scheme under various conditions. Additionally, a comprehensive examination of the simulation results is presented in Table 4.3. This analysis offers a detailed insight into the system's behavior, shedding light on key performance metrics and providing a solid foundation for understanding the effectiveness and feasibility of the proposed control scheme.

**Table 4.2** Nominal parameters and parasitic values of buck converter

| Parameter | Nominal value | Parasitic value |
|---|---|---|
| L- Inductor | 550 $\mu$H | $r_L$-150 m$\Omega$ |
| C- Capacitor | 10 $\mu$F | $r_c$ - 1$\Omega$ |
| R- Load resistor | 5 $\Omega$ | - |
| MOSFET | - | $R_{DS(ON)}$ – 3 m$\Omega$, $V_{SD}$ – 0.7 V |
| Diode | - | $V_d$ – 0.4 V |
| $V_{in}$ | 12 V | - |
| $V_{ref}$ | 5 V | - |
| $f$ | 25 kHz | - |

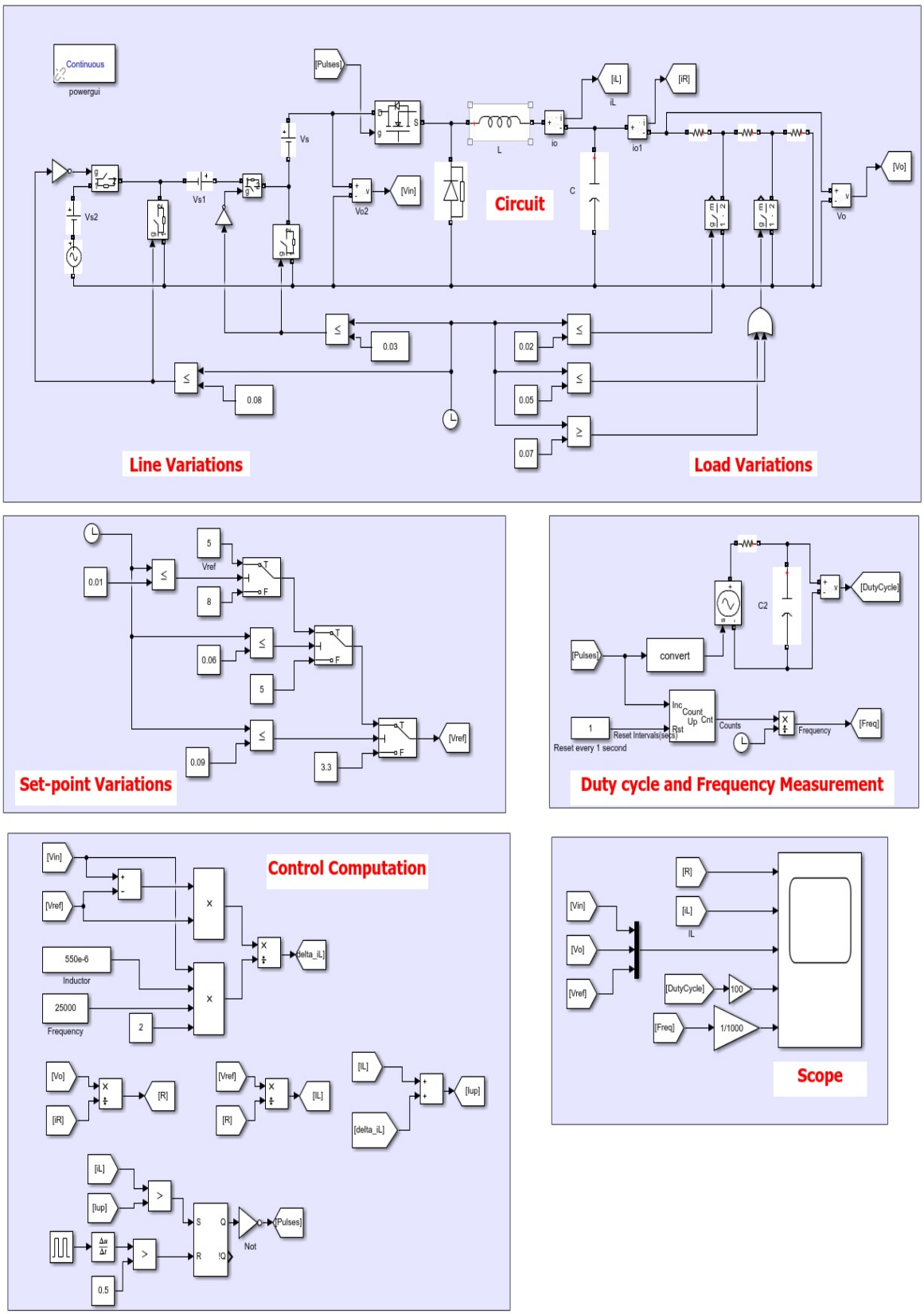



**Figure 4.5** SIMULINK layout of boundary-based PWM control scheme for buck converter simulation

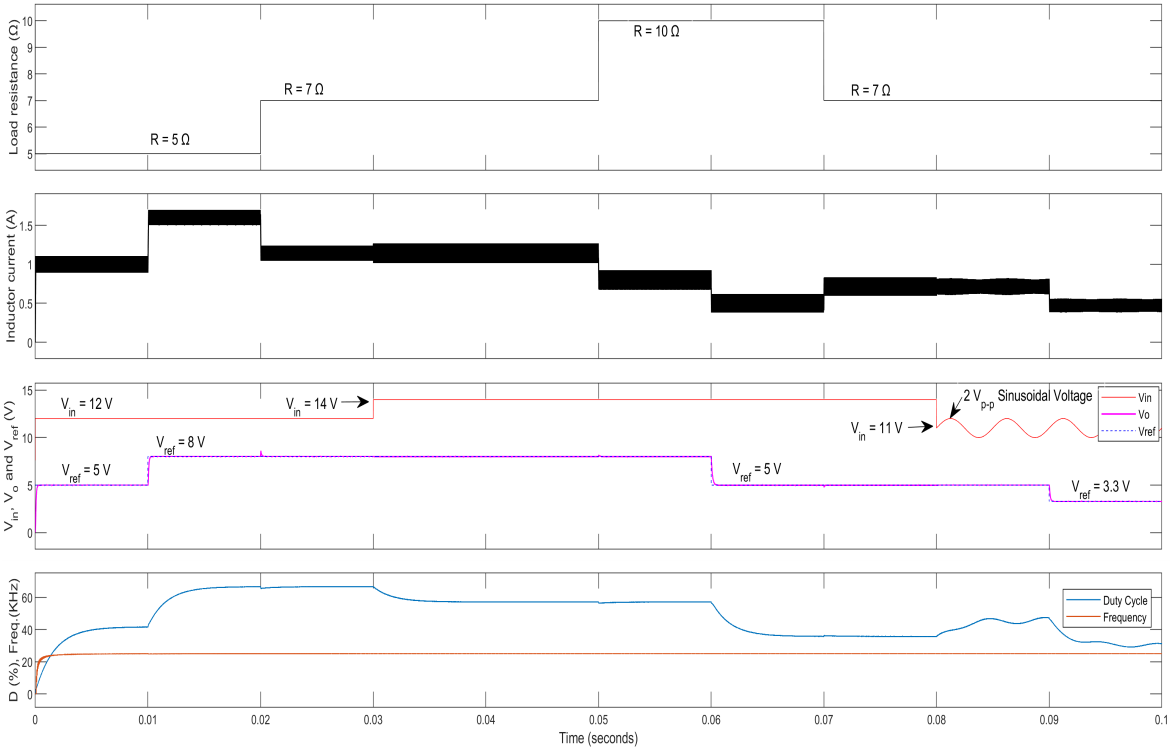


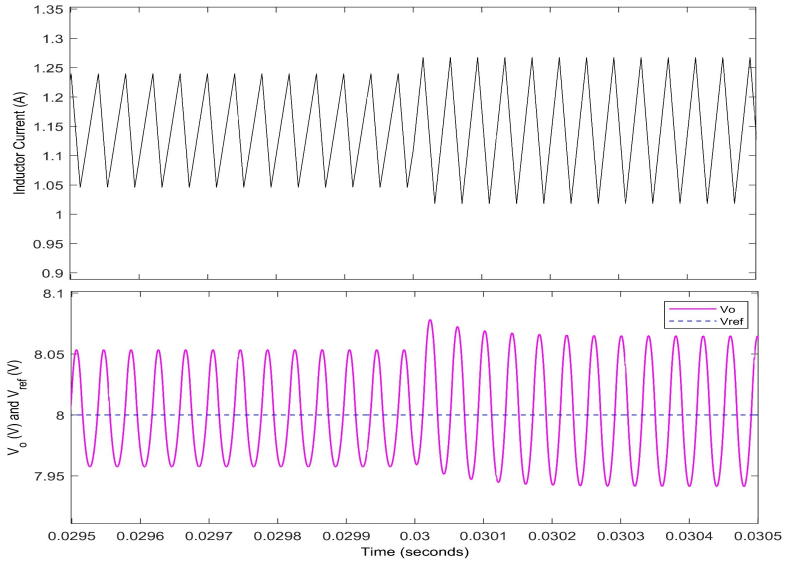

**Figure 4.6** Simulation outcomes for the boundary-based PWM control scheme applied to a buck converter, showcasing variations in **(a)** load resistance, **(b)** inductor current, **(c)** input voltage (red), reference voltage (blue), and output voltage (pink), and **(d)** frequency (red), duty cycle (blue)

**Table 4.3** $D$, $\%M_p$ , and $T_s$ analysis for buck converter under different scenarios

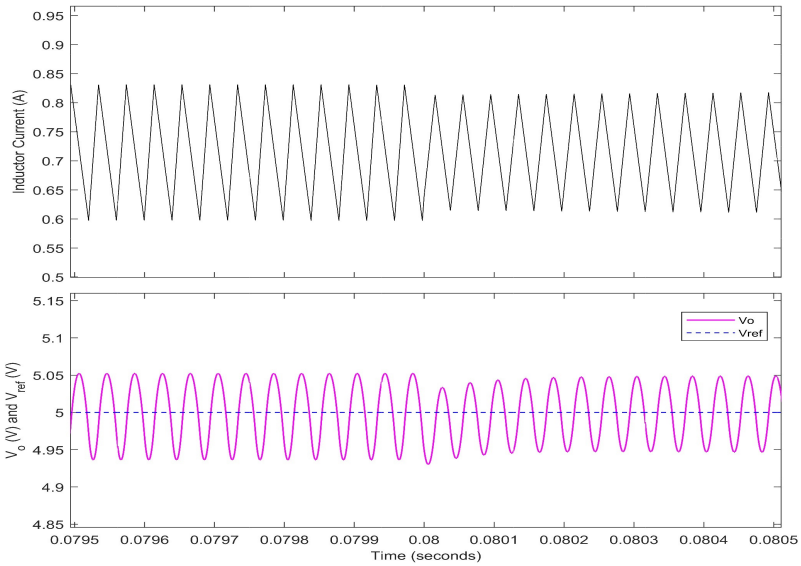
| Time span | $R$ | $V_{in}(V)$ | | $V_{ref}$ | $D$ | $\%M_p$ | $T_s$ | Problem |
|---|---|---|---|---|---|---|---|---|
| (s) | (Ω) | $V_{DC}(V)$ | $V_{AC}(V_{pp})$ | (V) | *(%)* | *(%)* | (ms) | |
| [0-0.01) | 5 | 12 | - | 5 | [0-41.5) | 1 | 0.3 | - |
| [0.01-0.02) | 5 | 12 | - | 5→8 | [41.5-66.5) | 0.6 | 0.3 | Servo: Set-point |
| [0.02-0.03) | 5→ 7 | 12 | - | 8 | [65.5-66.6) | 7.5 | 0.3 | Regulatory: Load |
| [0.03-0.05) | 7 | 12→14 | - | 8 | [66.6-57.2) | 1 | - | Regulatory: Input voltage |
| [0.05-0.06) | 7→10 | 14 | - | 8 | [56.3-57.2) | 2.5 | 0.4 | Regulatory: Load |
| [0.06-0.07) | 10 | 14 | - | 8→5 | [56.4-36.8) | 1.2 | 0.5 | Servo: Set-point |
| [0.07-0.08) | 10→7 | 14 | - | 5 | [36.2-36.7) | 4.8 | 0.3 | Regulatory: Load |
| [0.08-0.09) | 7 | 14→11 | 0→ 2 | 5 | [36.7-47.5) | 0 | - | Regulatory: Input voltage |
| [0.0-0.1) | 7 | 11 | 2 | 5→3.3 | [47.5-31.4) | 1.15 | 0.5 | Servo: Set-point |

### 4.4.1 Response to regulatory and servo problems

**Regulatory problem (Input voltage):** The findings displayed in Fig. 4.7 illustrate the controller's remarkable efficacy in addressing regulatory: input voltage challenges. Additionally, the simulation reveals that even when subjected to adverse conditions, such as a reduced input voltage of 11 V combined with the introduction of a sinusoidal voltage at $t$ = 0.08 sec, the controller consistently maintains stable output voltage levels without exhibiting any overshooting or undershooting tendencies. This outcome underscores the controller's resilience and trustworthiness in ensuring precise output voltage regulation, even when confronted with demanding operational scenarios.



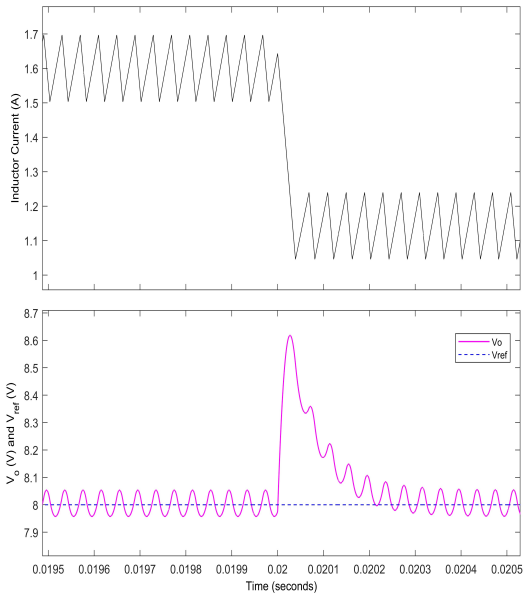

**(a)** $V_{in}$ variation: $V_{DC}$ (12 V to 14 V) at $t$ = 0.03 sec



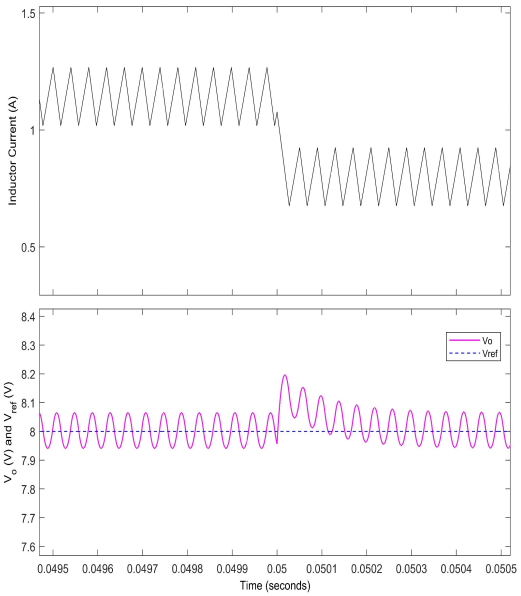

**(b)** $V_{in}$ variation: $V_{DC}$ (14 V to 11 V) and $V_{AC}$ (0 to $2V_{pp}$) at $t$ = 0.08 sec

**Figure 4.7** Transient response of buck converter state variables to line variations

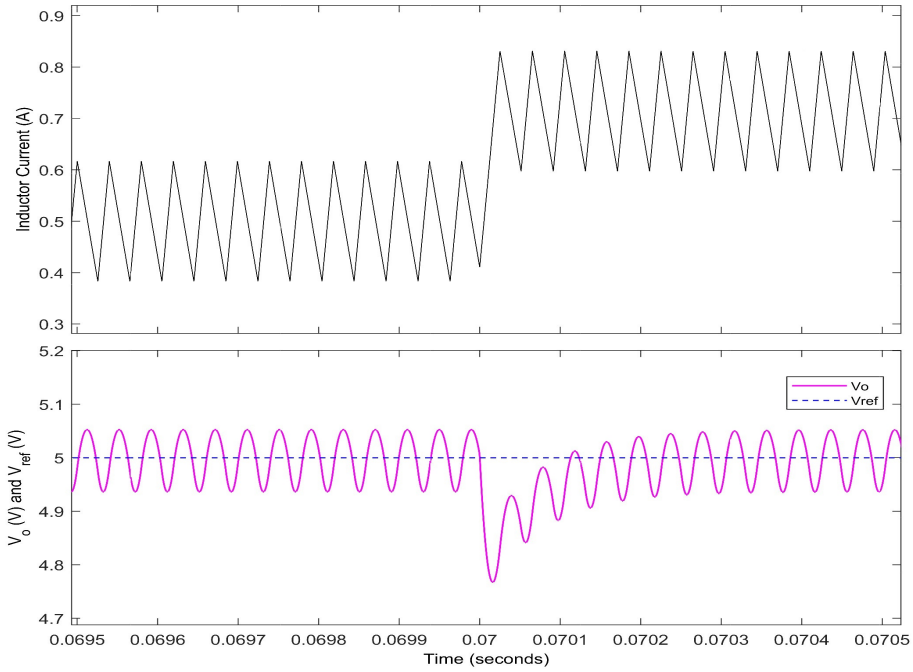
**Regulatory problem (Load):** Fig. 4.8 portrays the controller's reaction to different load disruptions, showcasing graphs of both inductor current and output voltage. Notably, at $t$ = 0.02 sec, when the load experiences a 40% increase and the set-point is raised by 60% compared to the nominal parameters, the system demonstrates a peak overshoot of 7.5%. This outcome highlights the controller's adeptness in mitigating the system's response to external disturbances, thereby guaranteeing that the output remains within acceptable thresholds.




**(a)** $R$ variation: 5 Ω to 7 Ω at $t$ = 0.02 sec



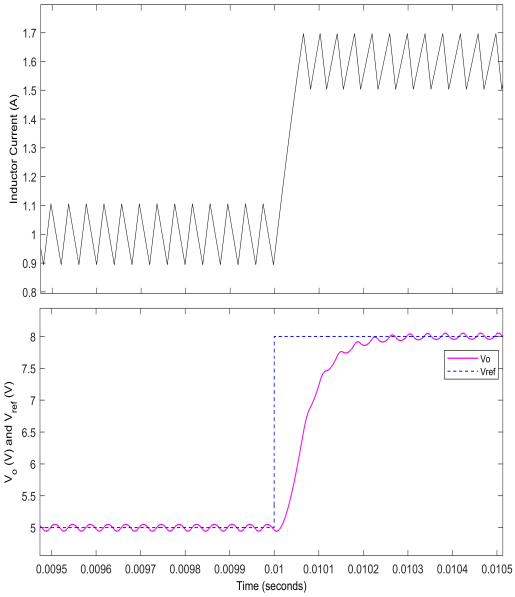

**(b)** $R$ variation: 7 Ω to 10 Ω at $t$ = 0.05 sec



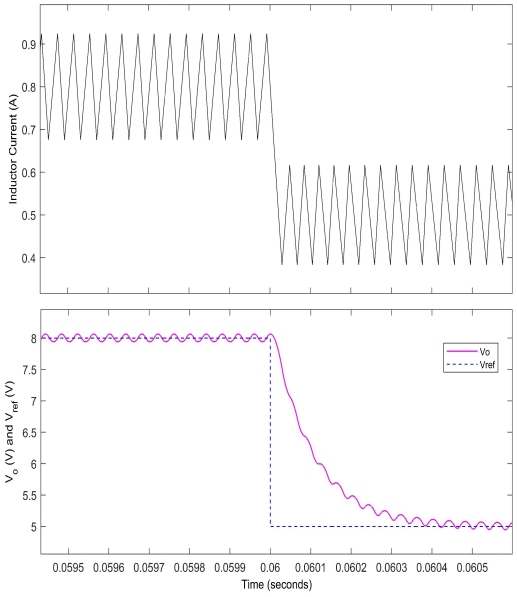

**(c)** $R$ variation: 10 Ω to 7 Ω at $t$ = 0.07 sec

**Figure 4.8** Transient response of buck converter state variables to load variations

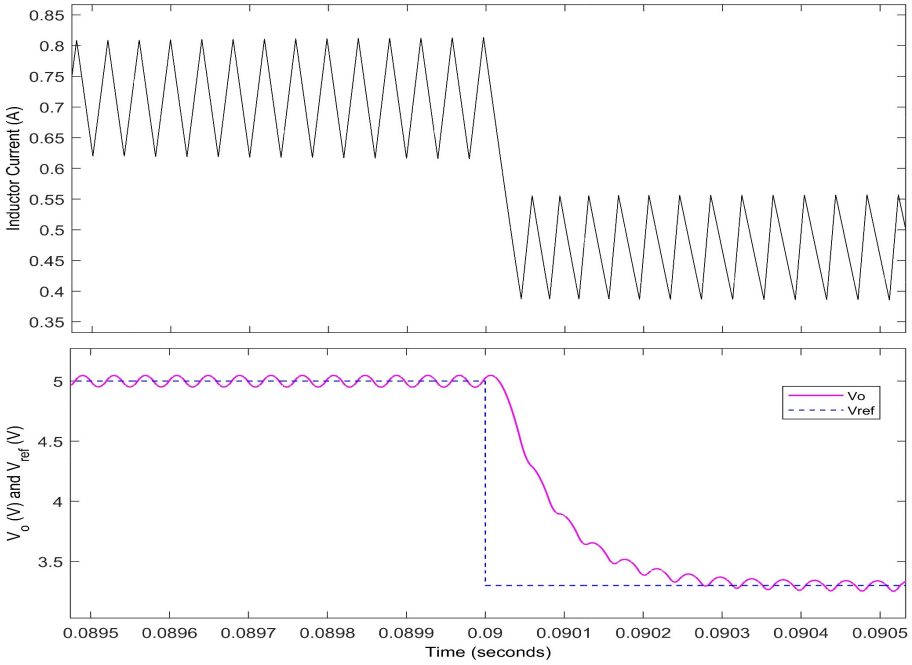
**Servo problem (Set-point tracking):** The findings showcased in Fig. 4.9 underscore the controller's exceptional performance in addressing servo-related challenges. The graphs provide clear evidence of the controller's ability to swiftly and precisely follow adjustments in the set-point, all while maintaining a remarkable absence of overshooting or undershooting. Notably, even when the set-point is lowered to 3.3 V in the presence of a sinusoidal input voltage, Fig. 4.6 and Fig. 4.9c illustrate how the output voltage continues to accurately track the reference signal, showcasing the controller's robust and reliable performance.




**(a)** $V_{ref}$ variation: 5 V to 8 V at $t$ = 0.01 sec




**(b)** $V_{ref}$ variation: 8 V to 5 V at $t$ = 0.06 sec




**(c)** $V_{ref}$ variation: 5 V to 3.3 V at $t$ = 0.09 sec

**Figure 4.9** Transient response of buck converter state variables to set-point variations

In summary, the simulation results unequivocally highlight the outstanding performance of the proposed controller in addressing both regulatory and servo control challenges. This controller consistently ensures stable output voltage with minimal to no overshooting or undershooting, affirming its excellence in handling a wide range of control scenarios.

### 4.4.2 Model mismatch analysis

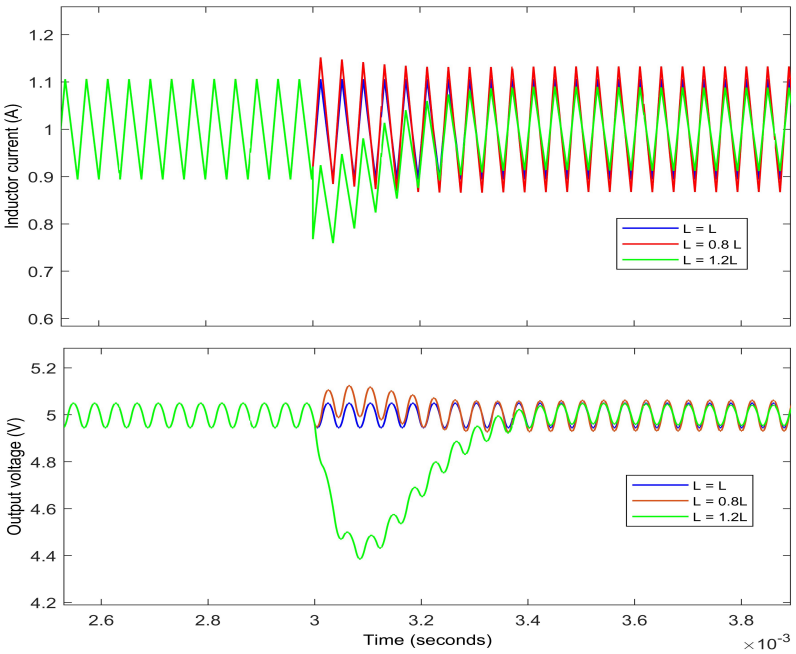
While the simulation outcomes are based on accurate SDS modeling, real-world circuits are vulnerable to a range of factors that can introduce inaccuracies, including variations in parameters and the presence of parasitic elements. Consequently, it becomes essential to assess the implications of these differences and explore possible strategies for minimizing their impact on the system's overall performance.

**Parametric variations:**

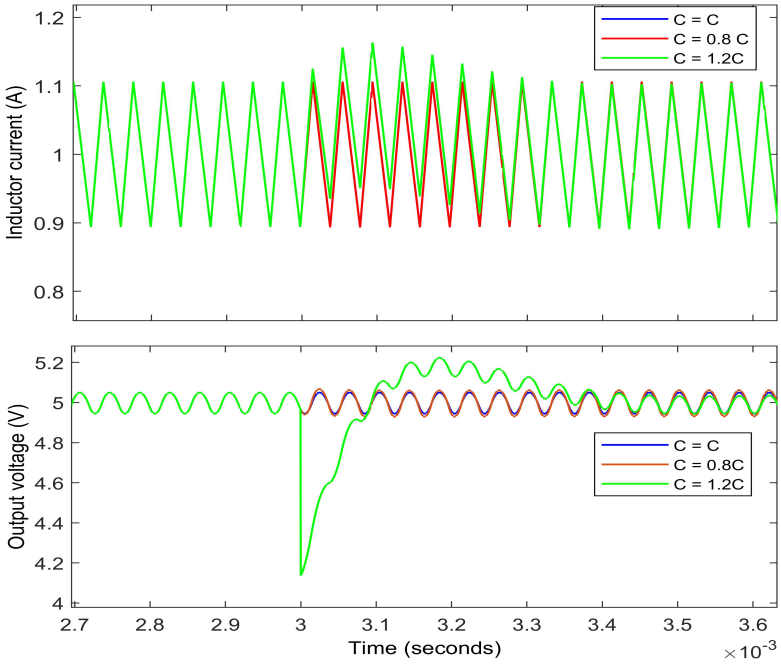
**Inductor:** A deviation of ±20% in the inductance value is introduced while keeping all other nominal parameters unchanged. According to (4.8), a reduction in the inductance value leads to an increase in $\Delta i_L$, as depicted in Fig. 4.10a. This occurs because, despite the reduced inductance, the inductor must still store the same amount of energy, necessitating an increase in current to maintain energy storage. The consequence of this change is a slight overshoot in the output voltage, attributable to the elevated $\Delta i_L$. Conversely, an increase in the inductance value results in a reduced $\Delta i_L$, as evident from Fig. 4.10a. Although an initial undershoot is observable, it swiftly stabilizes to the set-point.

**Capacitor:** In Fig. 4.10b, it is evident that $\Delta i_L$ remains relatively consistent, even in the presence of a -20% fluctuation in capacitance value, while all other nominal parameters are held constant. However, a minor fluctuation is noticeable in $\Delta v_o$. This phenomenon can be attributed to the capacitor's discharge rate when the MOSFET is switched off, and its subsequent slower charge rate when the MOSFET is switched on. When the capacitance value is increased by 20%, a noticeable and abrupt dip in the output voltage becomes apparent. Nevertheless, it's important to note that this dip is typically transient and stabilizes within a timeframe of 0.4 ms, as demonstrated in Fig. 4.10b. The reason behind this dip lies in the fact that the larger capacitance takes more time to charge up, and correspondingly, the inductor requires more time to transfer energy to the capacitor. Consequently, the output voltage experiences a temporary decrease until the capacitor reaches its full charge state.

The simulation outcomes provide strong evidence that the controller demonstrates robustness when faced with the specified fluctuations in the converter's parameters. This showcases the controller's effectiveness in upholding system stability and ensuring consistent performance, even when confronted with variations in inductance and capacitance.




**(a)** ±20% inductance variations




**(b)** ±20% capacitance variations

**Figure 4.10** Analysis of buck converter with proposed scheme to parametric variations

### Parasitic parameters:

In real-world applications, components like inductors, capacitors, diodes, and MOSFETs possess distinct characteristics that demand careful consideration during circuit design. These characteristics encompass factors such as inherent resistance, forward voltage thresholds, and on-resistance. When crafting a controller for a system, these details need to be taken into account. The simulation results, as illustrated in Fig. 4.11, take into account the influence of

parasitic parameters detailed in Table 4.2. As depicted in Fig. 4.11, the presence of these parasitic parameters results in a noticeable steady-state error. To address and mitigate this error, an integral compensation approach is introduced as follows.

$$u = K_I \int (V_{ref} - v_o)dt \tag{4.12}$$

To formulate the ultimate expression for $J$, it is imperative to incorporate the compensation term $u$ into (4.10). The resulting compensation is visually represented in Fig. 4.4. In this particular scenario, unity integral gain is assumed.

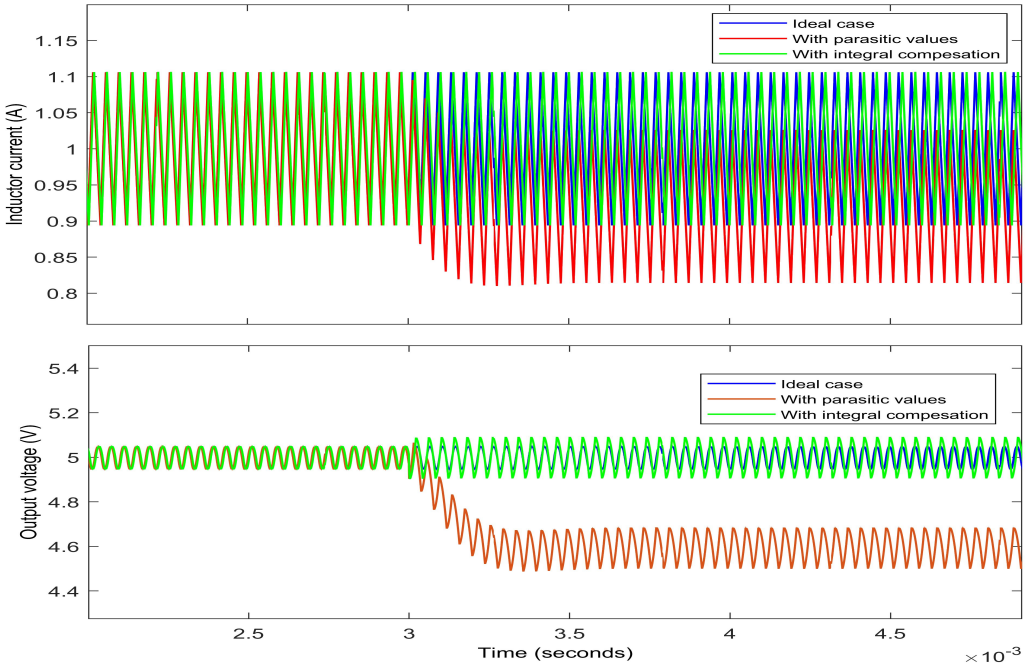



**Figure 4.11** Analysis of buck converter with proposed scheme with integral compensation to parasitic parameters

Through the application of the proposed current reference compensation technique, the controller retains its original structure and switching parameters. This ensures that the system maintains stable performance, even in the presence of unpredictable variations in system parameters. As demonstrated in Fig. 4.11, this approach significantly bolsters the system's overall resilience and robustness.

## 4.5 Comparative Analysis

Conducting a comparative analysis holds significant importance as it enables a comprehensive evaluation of various approaches. This analytical process facilitates the exploration of the unique strengths and limitations inherent to each approach, all within a consolidated framework. Such a thorough examination serves as a valuable tool for making well-informed decisions and tailoring solutions to meet specific requirements effectively.

The outlined design specifications are as follows: $V_{in}$ = 24 V, $L$ = 0.1 H, $C$ = 47 $\mu F$, $R$ = 25 Ω, $f$ = 5000 Hz, and $V_{ref}$ = 10 V [34]. Fig. 4.12 illustrates the waveforms of the state variables in accordance with the specified design criteria. Additionally, Table 4.4 provides a comparative analysis between the proposed control approach and the established PID and FOPID control schemes. This analysis highlights the distinctions and potential advantages of the proposed methodology.

The effectiveness of the proposed approach is notable in terms of enhancing rise time, reducing overshoot and undershoot, while also maintaining a high slew rate. It should be noted, however, that this method requires a longer settling time for the system to reach a steady-state value when compared to the FOPID scheme. Nonetheless, the advantages of improved performance justify the trade-off in settling time.

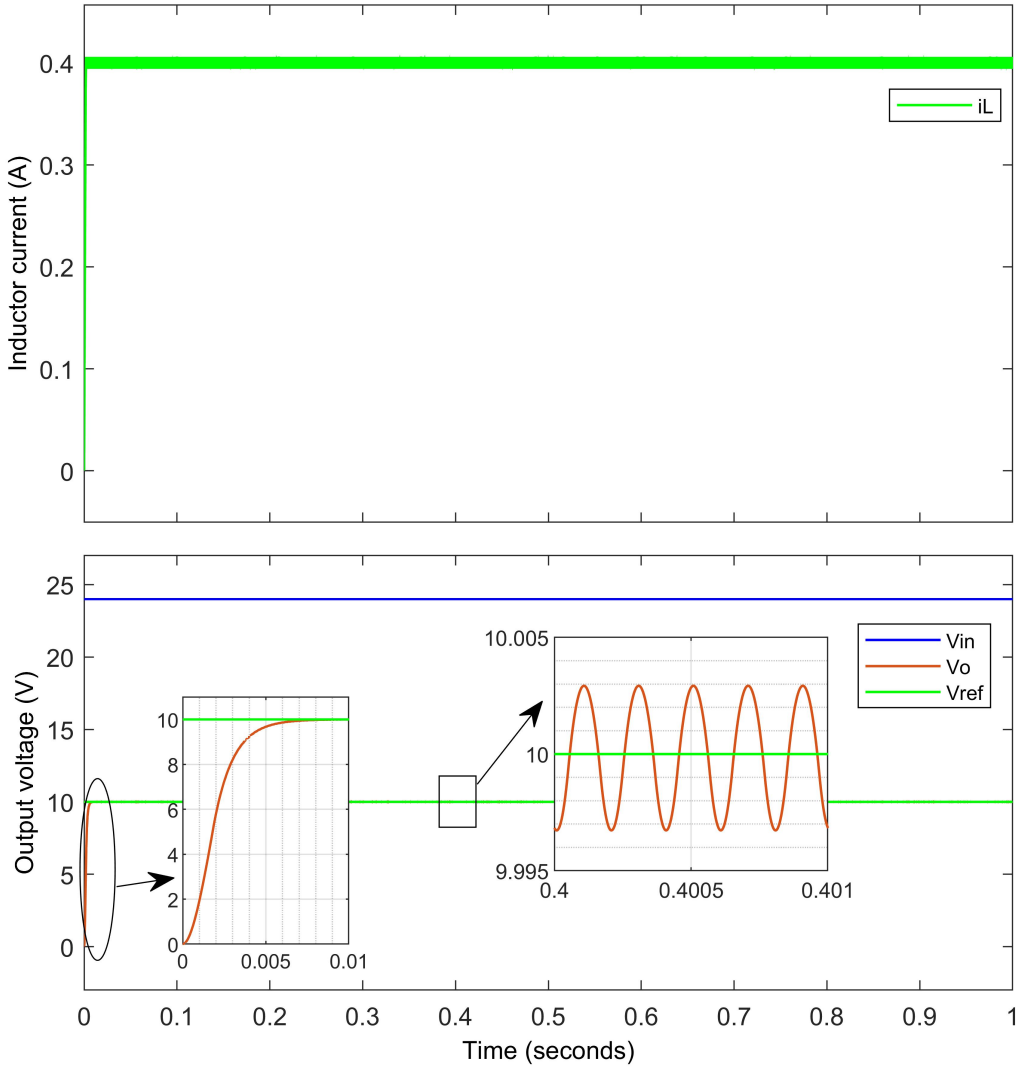



**Figure 4.12** Buck converter waveforms with proposed scheme for comparative analysis with PID and FOPID

**Table 4.4** Buck converter comparative performance evaluation: PID vs. FOPID vs. Proposed Scheme

| Parameter | PID [34] | FOPID [34] | Proposed scheme |
|---|---|---|---|
| $V_o$ (V) | 9.933 | 9.99 | **10** |
| Rise time ($\mu$s) | 92.687 | 40.614 | **2.943** |
| Slew rate (mV/ms) | 85.735 | 105.223 | **3863** |
| $\Delta\, v_o$ (V) | 0.02 | **0** | 0.006 |
| $M_p$ (%) | 15.698 | 0.505 | **0.503** |
| Undershoot (%) | 2 | 2.06 | **1.997** |
| $T_s$ (ms) | 19.98 | **0.003** | 3.535 |

## 4.6 Summary

In this study, the foundational principles and core operation of a buck converter are explored, employing state-space modeling techniques and hybrid automaton treating it as an SDS. A boundary-based PWM controller tailored for CCM is developed. Simulation results analyze regulatory and servo control challenges, demonstrating stable output voltage control. Model mismatch analysis considers component variations and parasitic parameters, addressing them with integral compensation. Comparative evaluation against PID and FOPID schemes showcases the superiority of the proposed approach in buck converter applications, affirming its effectiveness and resilience.

# CHAPTER-5

# Stability Analysis of Switched Dynamical System

Analyzing stability in SDSs is essential. Stability analysis aids in understanding system behavior, enabling reliable predictions and control. This analysis ensures safe and dependable operations in various applications, from robotics to power electronics. Examining stability in SDSs is crucial as it aids in detecting issues early and preventing larger complications. Without stability analysis, changes in the system can become erratic, potentially affecting functionality and safety. Thus, studying the stability of SDSs is imperative for robust and secure system design and operation. Consistent evaluation of this aspect is key for optimized performance and sustained reliability.

## 5.1 Stability Criteria and Theorems

Stability analysis of SDSs is a critical field in control theory and engineering. It examines the behavior of systems that can switch between different modes or subsystems. Ensuring stability in such systems involves assessing whether their trajectories converge or remain bounded over time. Researchers employ tools like Lyapunov stability theory to analyze the system's behavior and design control strategies to maintain stability [88][89][90]. This analysis is vital in various applications, including robotics, power systems, and communication networks, as it helps prevent undesirable oscillations or instability. Understanding the principles of stability in SDSs is essential for developing robust and reliable control systems.

The prevalent approach in stability analysis of SDSs entails the utilization of multiple Lyapunov functions [63][64][71]. This technique is rooted in the concept that, when Lyapunov functions are established for each continuous subsystem within the system, stability can be assured by placing particular constraints on the switching mechanism. Essentially, individually addressing the stability of each subsystem simplifies the overall stability analysis of the SDS and guarantees its dependable performance through controlled transitions between subsystems. This method streamlines the intricate task of evaluating the system's stability under switching conditions and improves the capacity to design robust control strategies.

Consider an SDS, $\dot{x}(t) = f(x(t), \sigma(t)) = f_{\sigma(t)}(x(t))$, where $\sigma(t)$ takes values from index set $M = \{1, \ldots, m\}$, and $m$ represents the number of subsystems. The stability of limit cycles can be demonstrated through the utilization of the method involving multiple Lyapunov functions.

**Theorem 1** *A family of Lyapunov-like functions is introduced and represented as* $\{V_\sigma, \sigma = 1, \ldots, m\}$, *each linked to the vector field* $f(x, \sigma) = f_\sigma(x)$. *A Lyapunov-like function associated with the system* $\dot{x} = f_\sigma(x)$ *and the equilibrium point* $x^* \in \Psi_\sigma \subset \mathbb{R}^n$ *is defined as a real-valued function* $V_\sigma(x)$, *applicable within the region* $\Psi_\sigma$. *It is subject to the following conditions:*

$$V_\sigma(x^*) = 0 \text{ and } V_\sigma(x) > 0 \text{ for } \forall x \in \Psi_\sigma \setminus \{x^*\} \tag{5.1}$$

Additionally, it is imperative that the Lyapunov function exhibits a derivative that is strictly negative definite. In alternative terms, (5.1) state that Lyapunov functions must be positive in their modes and have negative derivatives [7][91]. The transition between modes is controlled by an additional condition that guarantees the stability.

**Theorem 2** *Assume the existence of a constant, denoted as "*$\Upsilon$*" and greater than zero, such that for any pair of switching times,* $t_i$ *and* $t_j$, *where* $i < j$ *and* $\sigma(t_i) = \sigma(t_j)$, *the following condition holds:*

$$V_\sigma(t_j)(x(t_{i+1})) - V_\sigma(t_i)(x(t_{j+1})) \leq -\Upsilon |x(t_{i+1})|^2 \tag{5.2}$$

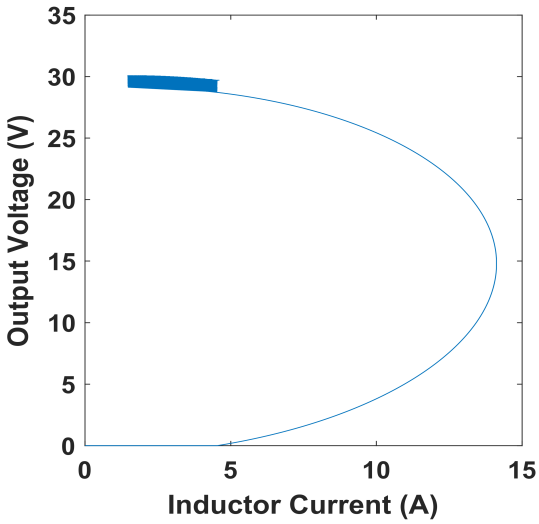
Based on the condition defined by (5.2), it can be established that the given SDS and switching function $\sigma(t)$ exhibits global asymptotic stability [92]. This implies that the system's state will eventually converge to a stable equilibrium point as time progresses. The term "Sawtooth Theorem" is attributed to this stability outcome due to the resemblance of typical energy profiles to a gradually diminishing sawtooth waveform when visualized [93].

To sum up, the utilization of the multiple Lyapunov function method imposes the requirement for distinct Lyapunov functions dedicated to each operational mode. These Lyapunov functions must rigorously demonstrate two fundamental properties, in accordance with Theorem 1: positivity and a decreasing trend. Furthermore, in line with the principles outlined in Theorem 2, these Lyapunov functions should exhibit a gradual reduction, akin to a diminishing sawtooth waveform.

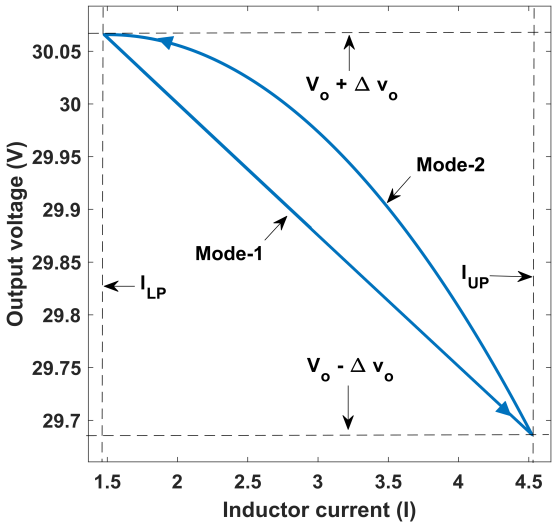
Therefore, by leveraging the insights provided by these theorems, the global asymptotic stability of the SDS can be conclusively determined. This implies that the system's behavior can be confidently assessed, and its tendency to converge towards a stable equilibrium state on a global scale can be confirmed.

## 5.2 Stability Assessment of Boost Converter Under Proposed Scheme

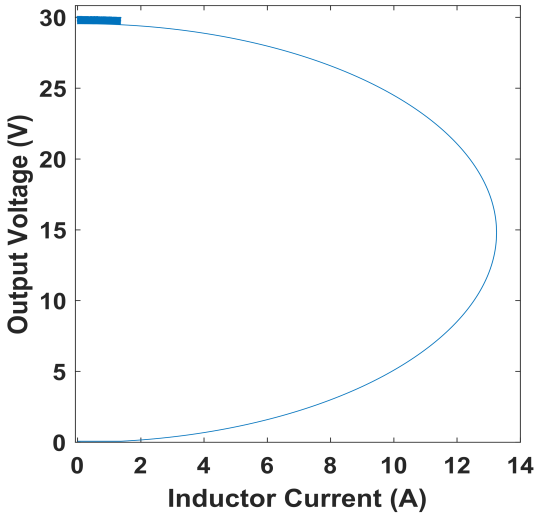
Analyzing the phase plane of a boost converter reveals distinct behaviors in both CCM and DCM. In CCM, the converter exhibits a continuous trajectory on the phase plane, as depicted in Fig. 5.1a and 5.1b. Conversely, DCM introduces additional complexity, with three phases: charging, discharging, and zero current, resulting in a more intricate trajectory illustrated in Fig. 5.1c and 5.1d. The proposed control scheme effectively navigates the system through these states in both modes, ensuring the emergence of a stable limit cycle. This limit cycle is of paramount importance for the analysis of SDSs, providing a basis for predicting and understanding the system's repetitive and predictable behavior. The stability of the boost converter, in conjunction with the proposed control scheme, will be scrutinized using multiple Lyapunov functions as a means of analysis, building upon the theorem mentioned earlier.



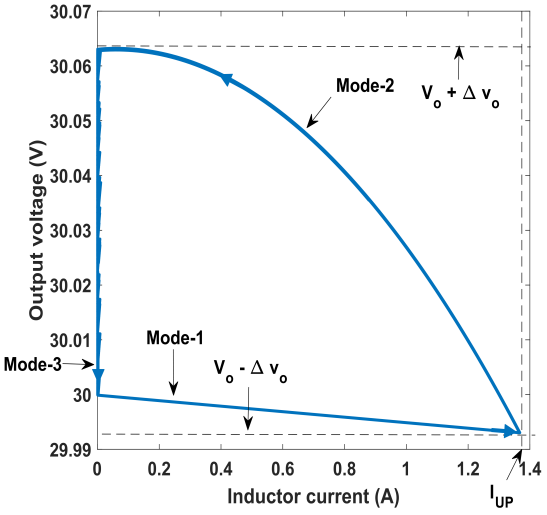

**(a)** State trajectories in CCM




**(b)** Limit cycle in CCM




**(c)** State trajectories in DCM




**(d)** Limit cycle in DCM

**Figure 5.1** Phase plane of boost converter with the proposed scheme

### 5.2.1 Analyzing stability in CCM of boost converter

There are two switching modes associated with the operation in CCM. The Lyapunov functions for each mode are defined as follows [94]:

- ***Mode-1:*** In this mode, the Lyapunov function is denoted as the energy function $L_1$, and it is expressed as follows:

$$L_1 = \frac{1}{2}L(I_{UP} - i_L)^2 + \frac{1}{2}C(V_o + \Delta v_o - v_o)^2 \tag{5.3}$$

  As this function is quadratic, it inherently remains positive, indicated by $L_1 > 0$. Moreover, its derivative exhibits a negative trend, as demonstrated below:

$$\frac{dL_1}{dt} = -\left[(I_{UP} - i_L)V_{in} + (V_o + \Delta v_o - v_o)\frac{v_o}{R}\right] \tag{5.4}$$

  Where,

$$\begin{cases} I_{UP} > i_L \implies (I_{UP} - i_L)V_{in} > 0 \\ (V_o + \Delta v_o - v_o) > 0 \implies (V_o + \Delta v_o - v_o)\dfrac{v_o}{R} > 0 \end{cases}$$

  Consequently, it becomes evident that this energy function $L_1$ maintains its positivity and demonstrates a decreasing trend. Therefore, $L_1$ qualifies as a Lyapunov function for mode-1.

- ***Mode-2:*** The energy function assigned to this mode is represented as $L_2$, and its expression is as follows:

$$L_2 = \frac{1}{2}L(i_L - I_{LP})^2 + \frac{1}{2}C(V_o + \Delta v_o - v_o)^2 \tag{5.5}$$

  This function exhibits positivity and its derivative is expressed as follows:

$$\frac{dL_2}{dt} = -\left[(i_L - I_{LP})(V_o - V_{in}) + (V_o + \Delta v_o - v_o)\frac{v_o}{R}\right] \tag{5.6}$$

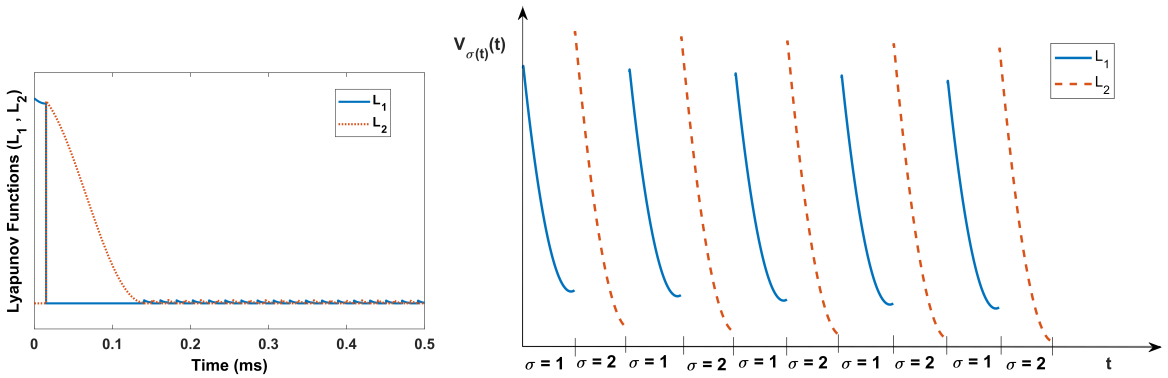
  Where,

$$\begin{cases} i_L > I_{LP} \implies (i_L - I_{LP})(V_o - V_{in}) > 0 \\ (V_o + \Delta v_o - v_o) > 0 \implies (V_o + \Delta v_o - v_o)\dfrac{v_o}{R} > 0 \end{cases}$$

  Therefore, this function remains positive and exhibits a declining trend throughout this mode. Consequently, $L_2$ qualifies as a Lyapunov function for mode-2.

In each CCM operational mode, all Lyapunov functions exhibit two essential characteristics: they are always positive (non-negative) and consistently decrease over time, satisfying (5.1). As a result, in the CCM, the validation of Theorem-1 is confirmed.

The next step involves a comprehensive exploration of Theorem-2, which necessitates the plotting of the Lyapunov functions. The (5.2) serves as a critical criterion for ensuring that the switching process maintains the system's overall stability when moving from one mode to another. Fig. 5.2 illustrates the evolution of Lyapunov functions for CCM. This figure serves as a valuable tool for evaluating the global asymptotic stability of the system. The visual representation clearly shows that the Lyapunov functions display a gradually decreasing sawtooth pattern. This visual proof strongly supports the global asymptotic stability of the boost converter based on the proposed approach for CCM as described in (5.2).




**(a)** Evolution overtime **(b)** Enlraged view

**Figure 5.2** Evolution of Lyapunov functions for boost converter with proposed scheme in CCM

### 5.2.2 Analyzing stability in DCM of boost converter

There are three switching modes associated with the operation in DCM. The Lyapunov functions for each mode are defined as follows [94]:

- ***Mode-1:*** For this purpose, the same $L_1$ used in mode-1 for CCM is chosen. Consequently, the conditions can be validated. The only variation lies in the value assigned to $I_{UP}$ for CCM and DCM, but these differences have no impact on the overall equation.

- ***Mode-2:*** In this mode, the energy function is denoted as $L_2$, and its expression is as follows:

$$L_2 = \frac{1}{2}L(i_L)^2 + \frac{1}{2}C(V_o + \Delta v_o - v_o)^2 \tag{5.7}$$

  This function maintains positivity and its derivative is given by:

$$\frac{dL_2}{dt} = -\left[(i_L)(V_o - V_{in}) + (V_o + \Delta v_o - v_o)\frac{v_o}{R}\right] \tag{5.8}$$

Where,

$$\begin{cases} i_L > 0 \implies (i_L)(V_o - V_{in}) > 0 \\ (V_o + \Delta v_o - v_o) > 0 \implies (V_o + \Delta v_o - v_o)\dfrac{v_o}{R} > 0 \end{cases}$$

Hence, this function sustains its positivity and demonstrates a decreasing pattern. As a result, $L_2$ is considered a Lyapunov function for mode-2.

- ***Mode-3:*** In mode-3, where the inductor current is zero, the energy function for this mode can be defined as follows:

$$L_3 = \frac{1}{2}C(V_o + \Delta v_o - v_o)^2 \tag{5.9}$$

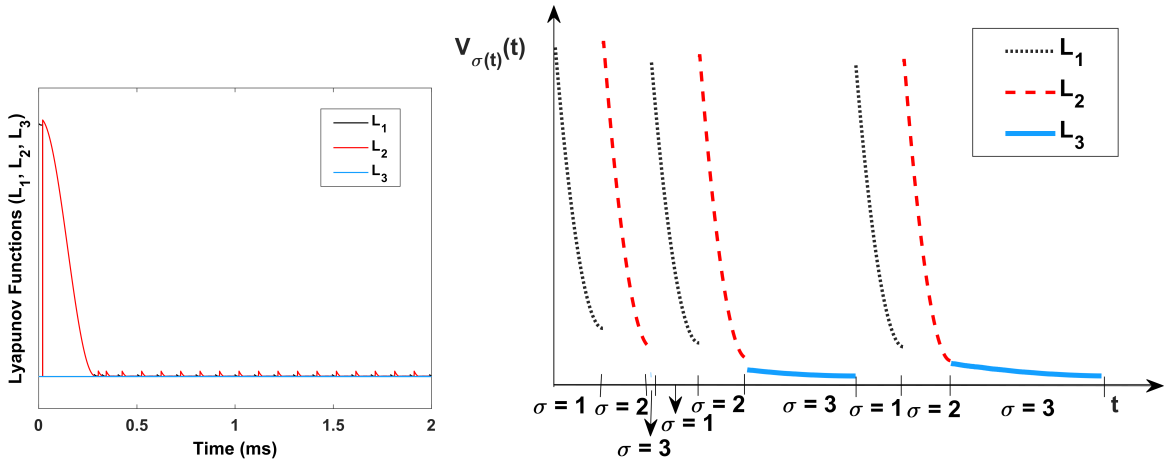
This function is inherently positive. Its derivative is expressed as follows:

$$\frac{dL_3}{dt} = -\left[(V_o + \Delta v_o - v_o)\frac{v_o}{R}\right] \tag{5.10}$$

Consequently, the derivative of $L_3$ remains consistently negative. This characteristic renders $L_3$ suitable for mode-3.

So, in each operational mode of the DCM, it is essential to note that all Lyapunov functions possess two characteristics: they are always non-negative and they exhibit a continuous decrease over time, as described by (5.1). Therefore, in DCM as well, the validation of Theorem-1 is affirmed.

Now, similar to analysis in CCM, attention is turned to DCM to assess Theorem-2. A visual representation of the evolving Lyapunov functions is provided in Fig. 5.3. The observed waveforms of these functions exhibit a consistent downward trend, resembling a gradually




**(a)** Evolution overtime **(b)** Enlraged view

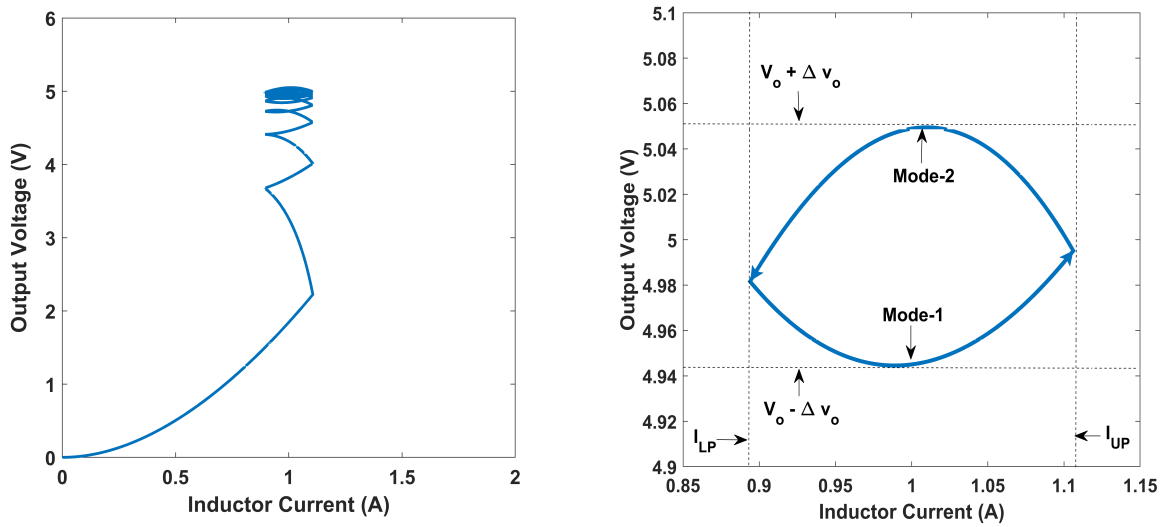
**Figure 5.3** Evolution of Lyapunov functions for boost converter with proposed scheme in DCM

decreasing sawtooth pattern. This observation leads to the confirmation of global asymptotic stability, which is supported by the validation of (5.2) for the boost converter in DCM.

In summary, the validation of both theorems in both CCM and DCM reaffirms the stability of the boost converter under the proposed scheme.

## 5.3 Stability Assessment of Buck Converter Under Proposed Scheme

Understanding the phase plane shows different behaviors in the buck converter. When it works in CCM, the converter follows a continuous path on the phase plane, as shown in Figure 5.4. The proposed control strategy effectively guides the system through these states, making sure a stable repeating pattern, called a limit cycle, happens. This limit cycle is crucial for studying SDSs because it aids in predicting and understanding how the system repeats predictably. To determine the stability of the buck converter in CCM, multiple Lyapunov functions will be employed for analysis, which is built upon the earlier-mentioned theorem.




**(a)** State trajectories **(b)** Limit cycle

**Figure 5.4** Phase plane of buck converter with the proposed scheme in CCM

There are two distinct switching modes linked to the operation in CCM. The Lyapunov functions for each mode are defined as follows [91]:

- ***Mode-1:*** In this mode, the Lyapunov function is denoted as the energy function $L_1$, and it is expressed as follows:

$$L_1 = \frac{1}{2}L(I_{UP} - i_L)^2 + \frac{1}{2}C(V_o + \Delta v_o - v_o)^2 \tag{5.11}$$

  Since this function is quadratic in nature, it inherently maintains a positive value, as evidenced by $L_1 > 0$. Furthermore, its derivative displays a decreasing trend, as shown

below:

$$\frac{dL_1}{dt} = -\left[(I_{UP} - i_L)(V_{in} - V_o) + (V_o + \Delta v_o - v_o)\frac{v_o}{R}\right] \tag{5.12}$$

Where,

$$\begin{cases} (I_{UP} > i_L)\ and\ (V_{in} > V_o) \implies (I_{UP} - i_L)(V_{in} - V_o) > 0 \\ (V_o + \Delta v_o - v_o) > 0 \implies (V_o + \Delta v_o - v_o)\dfrac{v_o}{R} > 0 \end{cases}$$

As a result, it becomes clear that this energy function, denoted as $L_1$, not only stays positive but also exhibits a decreasing trend. Thus, $L_1$ fulfills the criteria to be considered a Lyapunov function for mode-1.

- ***Mode-2:*** The energy function designated for this mode is denoted as $L_2$, and its expression is as follows:

$$L_2 = \frac{1}{2}L(i_L - I_{LP})^2 + \frac{1}{2}C(V_o + \Delta v_o - v_o)^2 \tag{5.13}$$

This function exhibits positivity and its derivative is expressed as follows:

$$\frac{dL_2}{dt} = -\left[(i_L - I_{LP})V_o + (V_o + \Delta v_o - v_o)\frac{v_o}{R}\right] \tag{5.14}$$

Where,

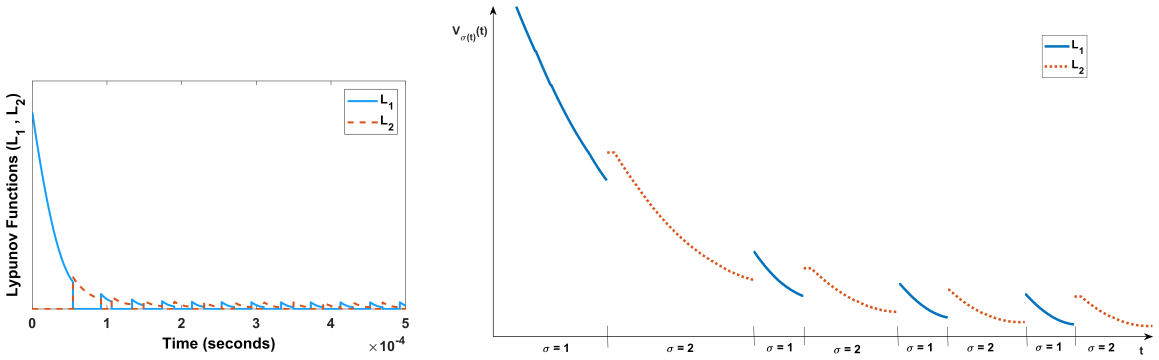
$$\begin{cases} i_L > I_{LP} \implies (i_L - I_{LP})V_o > 0 \\ (V_o + \Delta v_o - v_o) > 0 \implies (V_o + \Delta v_o - v_o)\dfrac{v_o}{R} > 0 \end{cases}$$

Hence, this function maintains a positive value and demonstrates a decreasing pattern. Consequently, $L_2$ satisfies the criteria to be considered a Lyapunov function for mode-2.

Thus, within each operational mode, all Lyapunov functions showcase two essential traits: positivity, indicating their non-negativity, and a decreasing trend, signifying their continuous reduction over time which satisfies (5.1). This dual attribute validates the system's stability across CCM.

To examine the stability of transitions between modes, it is crucial to assess (5.2) by generating plots depicting the waveforms of Lyapunov functions. These equations play a pivotal role in guaranteeing that switching operations uphold the stability of the system. Fig. 5.5 shows Lyapunov function evolution in CCM, aiding in evaluating global asymptotic stability. The graphical representation provides strong evidence by showing that Lyapunov functions consistently follow a pattern resembling a gradually decreasing sawtooth. This pattern confirms

that the buck converter, as operated under the proposed scheme, is globally asymptotically stable.




**(a)** Evolution overtime **(b)** Enlraged view

**Figure 5.5** Evolution of Lyapunov functions for buck converter with proposed scheme in CCM

In brief, the confirmation of both theorems underscores the stability of the buck converter with the suggested approach.

## 5.4 Summary

Ensuring stability in SDS systems is vital for control strategy validation. The use of multiple Lyapunov functions is a common method, with theorems playing a crucial role in proving global asymptotic stability. The proposed approach applies to both boost and buck converters, demonstrating global asymptotic stability through compliance with Lyapunov function conditions. Graphs of these functions enhance clarity. The approach successfully establishes stability for both converters, supported by thorough Lyapunov function analysis. This robust confirmation enhances system reliability and underscores the control strategy's effectiveness.

# CHAPTER-6

# Controller Realization on FPGA Board using MBD Approach

Controller realization using MBD is essential for efficiently developing and implementing control systems by leveraging mathematical models and simulations to ensure accuracy and reliability while reducing development time and costs. MBD is a systematic approach used in engineering, particularly in fields like aerospace, automotive, and control systems. It involves creating mathematical or computational models to represent a system's behavior. These models are then used for simulation, testing, and even automatic code generation. MBD enables rigorous verification and validation, fostering an iterative design process and facilitating collaboration among multidisciplinary teams. It's especially valuable in safety-critical industries, ensuring reliability and reducing costs by catching design flaws early. Overall, MBD enhances system reliability, reduces development costs, and speeds up time-to-market in complex engineering projects.

In the domain of MBD, the integration of FPGA through the FIL approach has emerged as a powerful and versatile technique [78]. This method seamlessly combines hardware and software development to validate and test control algorithms and system models in real-time on FPGA hardware [74]. FPGAs offer significant advantages in terms of speed and parallel processing capabilities, making them ideal for rapid prototyping and testing of complex control systems. With the FIL approach, SIMULINK models can directly be interfaced with FPGA, facilitating a closed-loop environment for testing and verification [77].

This approach not only accelerates the development process but also ensures a higher degree of confidence in the final system's performance. It is particularly valuable in safety-critical applications, such as automotive control systems and aerospace avionics, where real-time validation is paramount. By harnessing the synergy between MBD and FPGA technology, the design workflow is streamlined, development time is reduced, and more robust and efficient control systems are ultimately delivered.

Through the application of MBD and the FIL technique, the proposed control strategies for

boost and buck converters are implemented and rigorously validated. This validation process ensures the effectiveness and reliability of the controllers in regulating the operation of these vital power electronic devices.

## 6.1 MBD Workflow

MBD offers an effective method to establish a unified communication framework throughout the design process while aligning with the development cycle, often referred to as the V-model [73]. When applied to control system design, this approach manifests in a sequence of four distinct developmental stages [95] [96].

**Model-in-the-Loop (MIL):** MIL testing is a crucial step in control system verification and validation. It involves creating a controller that works effectively with a simulated plant model to predict real-world behavior. MIL testing is iterative, starting with a simplified model and gradually refining it for accuracy. High-uncertainty elements are prioritized for detailed development to cover challenging scenarios. This raises technology readiness early when changes are cost-effective. When MIL results meet requirements, development progresses. This systematic approach enhances control system reliability and effectiveness, reducing unexpected issues in real-world deployment.

**Software-in-the-loop (SIL):** SIL testing is a critical step in engineering and software development. After converting the control model into code, SIL testing aims to identify and correct errors. It involves running the generated C code on a local computer and comparing it to results from MIL testing. Any discrepancies suggest issues in the code or model, requiring investigation. When MIL and SIL results match after adjustments, it signals a smooth development process, allowing the project to progress further. SIL testing ensures software code aligns with the control model, maintaining quality in engineering and software development.

**Processor-in-the-loop (PIL):** PIL testing is a vital phase in system verification and validation. It follows MIL and SIL testing. PIL comes into play after compiling and deploying C code from the system model onto the target microcontroller or FPGA. PIL's main aim is to ensure the compiled code operates correctly on the intended processor. This involves running the processor while connected to a plant model simulating the system. The goal is to confirm the processor can execute control logic and tasks as required in the real world.

PIL testing can also apply to an FPGA, known as FIL testing [97]. This assesses code for optimal performance on an FPGA. Results from PIL/FIL tests are compared to SIL results, a critical checkpoint. Discrepancies signal potential issues in the model, code, or processor setup. Addressing these discrepancies ensures a robust and dependable system, allowing for

confident progress in development.

**Hardware-in-the-Loop (HIL):** HIL testing is a crucial phase in the development and testing of complex systems, particularly in aerospace, automotive, and industrial automation. It acts as the final check before integrating the system and conducting human-involved end-to-end testing. During HIL testing, control software runs on a real-time hardware platform such as dSpace, National Instruments PXI, MathWorks SIMULINK Real-Time, Speedgoat Real-Time Target Machines, Opal-RT, ETAS LABCAR, or Typhoon HIL, simulating the actual operational environment. Key elements include the real-time system for rapid computations, a plant model mimicking the physical system, physical connections mirroring real-world setups, and testing of communication protocols. The terms FIL and HIL are sometimes used interchangeably, but they do have distinct meanings and applications. FIL emphasizes the use of FPGA technology for real-time simulation and testing, whereas HIL encompasses a broader range of hardware elements and is focused on testing control systems with real hardware.

HIL testing's primary goal is to uncover communication and interface issues early, comparing results with prior testing stages to ensure consistency. When all stages align, it indicates control system readiness for production, ensuring a reliable and consistent performance in the field. This process is an essential quality assurance step in complex system development.

## 6.2 MATLAB/SIMULINK and FIL

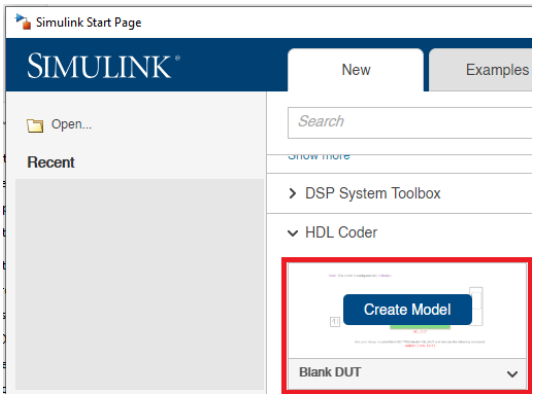
In the dynamic landscape of MATLAB/SIMULINK, where engineering innovation converges with simulation prowess, a formidable tool takes the spotlight - Hardware Description Language (HDL) Workflow Advisor. The HDL Workflow Advisor and FIL play crucial roles within the realm of control system design and electronic engineering, particularly in the context of FPGA development. The HDL Workflow Advisor serves as a guiding system, overseeing the design process, identifying errors, optimizing designs, producing documentation, and ensuring compatibility with various HDL languages. Conversely, FIL facilitates early testing, real-world simulation, debugging, and verification, playing a vital role in the development of safety-critical systems in FPGA design, rendering it an indispensable tool. These elements collaboratively elevate efficiency and dependability in the development of electronic control systems. The process of implementing the FIL technique is elaborated upon in the subsequent content, providing a comprehensible and step-by-step direction.

### 6.2.1 FIL simulation using HDL Workflow Advisor in SIMULINK

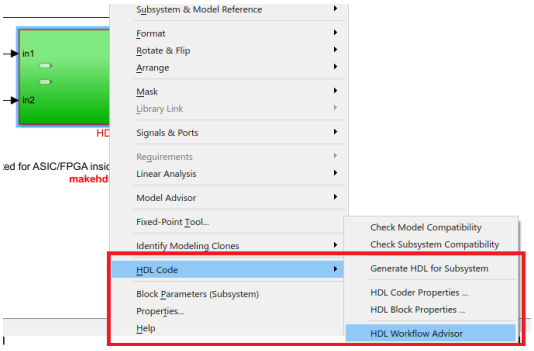
To utilize FIL with MATLAB/SIMULINK, specific hardware and software components are necessary. These include an FPGA board, the corresponding Design Suite software for

selected FPGA board, HDL Coder, and any additional toolkits that are required based on the specific program's needs. The procedure for performing FIL simulations using the HDL Workflow Advisor in SIMULINK is described as follows [98].

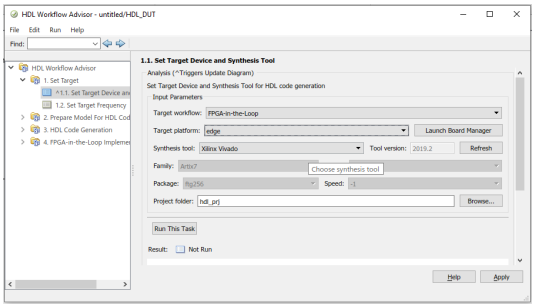
- Begin by launching MATLAB and opening SIMULINK. In SIMULINK, navigate to the "HDL Coder" section and choose "Blank DUT," as depicted in Fig. 6.1a.
- The next step involves designing the controller within the HDL_DUT subsystem, while placing all other components in the SIMULINK environment.
- Once the controller design within the HDL_DUT block is completed, proceed by right-clicking on the HDL_DUT block. Then, select "HDL Code" and subsequently choose "HDL Workflow Advisor." This sequence of actions will open a screen resembling the one depicted in Fig. 6.1b.
- In the subsequent stages, there are four significant steps that need to be executed.
    1. In this critical step, the Target Workflow (FIL), Target Platform (Artix 7 FPGA board), and Synthesis Tool (Vivado, a Design Suite software from Xilinx) must be selected, as illustrated in Fig. 6.1c. Additionally, the Target Frequency (default 25 MHz) should also be specified.
    2. The subsequent step involves preparing the model for HDL code generation, comprising five substeps. Each substep must be verified by right-clicking on it and selecting "Run this task".
    3. Following that is the HDL code generation step, which should be verified as explained in Step 2.
    4. Lastly, in this step, the FIL options need to be validated, as discussed in Step 2. Here, FIL Connection is selected as JTAG. If the FPGA board is connected via Ethernet, then the Board IP address and Board MAC address must be specified. This step should also be verified, as in the previous steps.
    5. In summary, all four steps must be verified, indicated by a green checkmark as shown in Fig. 6.1d. If any errors are generated, they must be resolved; otherwise, the next step cannot proceed.
- Upon completing Step 4, the HDL Workflow Advisor generates a FIL block named after the top-level module and situates it in a new model, as depicted in Fig. 6.1e. Additionally, a Bitstream file is generated.
- To summarize, the generated Bitstream file should be loaded onto the FPGA board. This can be achieved by double-clicking on the generated FIL block and browsing for the file.



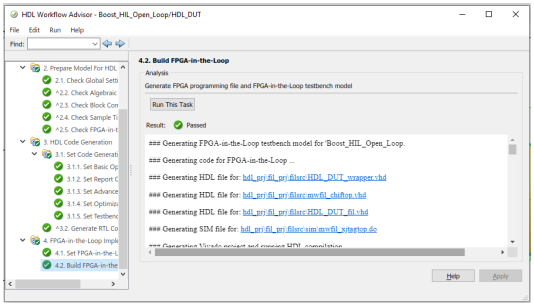

**(a)** Creating Blank DUT



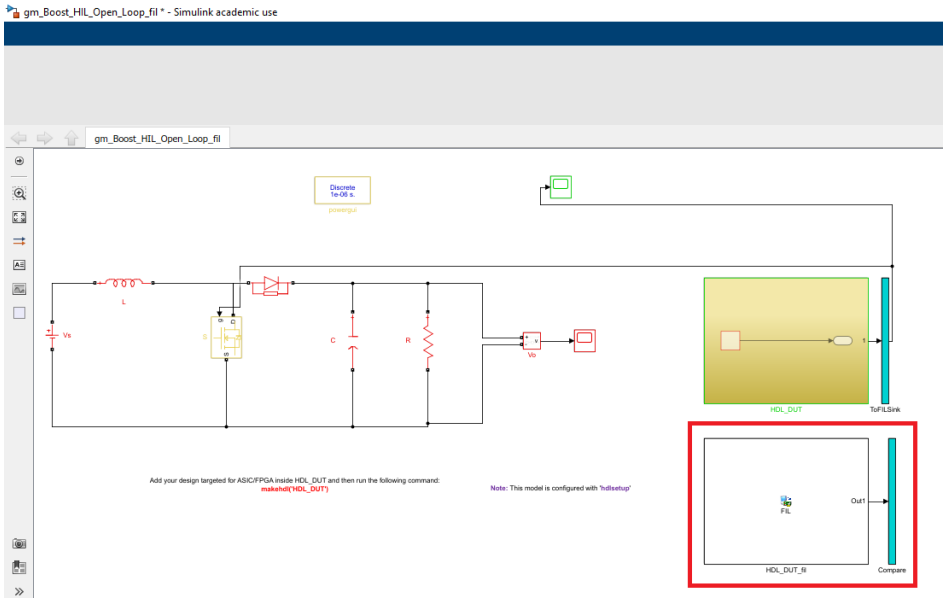

**(b)** Accessing HDL Code generation option




**(c)** Selection of Target and Platform for FIL




**(d)** Verification of Workflow steps




**(e)** Final Outcome: Generated FIL Block

**Figure 6.1** MATLAB/SIMULINK and FIL Workflow: Key Steps

Fig. 6.2 illustrates a flowchart that outlines the entire process of conducting a FIL simulation within the MATLAB/SIMULINK environment. This visual representation provides a structured overview of the sequential steps and interactions involved in the simulation.

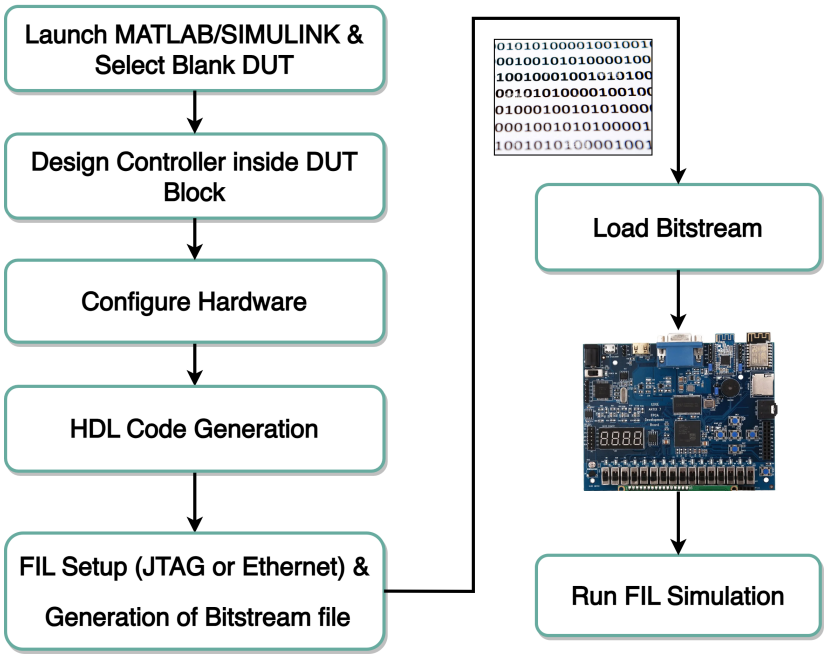



**Figure 6.2** Flowchart illustrating the FIL simulation process in MATLAB/SIMULINK

### 6.2.2 Artix 7 FPGA board and Vivado Design Suite

The Xilinx Artix 7 FPGA is chosen for the FIL application for its exceptional computational capabilities and versatility in enabling real-time control algorithm validation. Fig. 6.3 displays the Artix 7 board along with its various components. The board is equipped with essential hardware components to facilitate the validation of control algorithms through FIL. At its core, the Xilinx Artix 7 XC7A35T-1FTG256C FPGA, exhibits 33,208 logic elements and 1,843,200 bits of Block RAM, provides the necessary computational power for real-time control algorithm testing. Complementing the FPGA, a generous 32MB (256Mbit) SDRAM proves invaluable for data and program variable storage during algorithm validation, while a 64 Mb FLASH memory serves as a reliable FPGA configuration source. Data storage is simplified with MicroSD card support, while USB JTAG and USB UART interfaces enable programming, debugging, and communication. Moreover, the system operates seamlessly with a 50 MHz single-ended clock, ensuring the precision required for control algorithm validation.

While the following components may not currently be utilized in FIL, they still hold significant value for potential future expansions and enhancements. For seamless data exchange, the system offers both an ESP-12F WiFi modem and Bluetooth BLE 4.0 interfaces. These capabilities allow for flexible deployment of control algorithms and data retrieval. Additionally, the system supports visual feedback and monitoring with a 12-bit VGA output featuring 4096 colors and HDMI output. These display options empower users to visualize control system behavior in

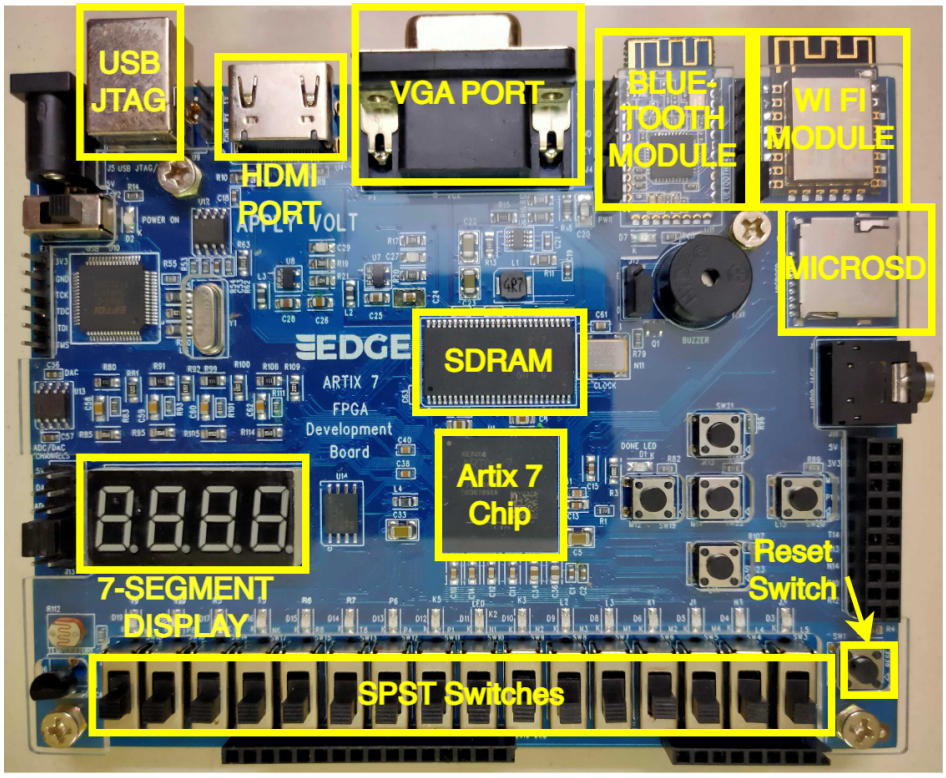



**Figure 6.3** The Artix 7 FPGA Board

real-time. Sensors, including an LM35 Temperature Sensor and an LDR (Light Dependent Resistor), are integrated for data acquisition, complemented by a 12-bit SPI DAC output for analog signal generation. Audio feedback is facilitated through a stereo jack and a 5V Piezo Buzzer, and numerical and text-based information display is enhanced with a 4-digit 7-segment display and a 2×16 character LCD screen. User interaction is enabled through 16 SPDT slide switches, 16 LEDs, and 5 push buttons, facilitating control over algorithm parameters and system response observation. In summary, the Artix 7 FPGA Board is a potent device suitable for conducting FIL simulations.

Vivado, developed by Xilinx, is a crucial Integrated Development Environment (IDE) for FPGA design. Although not directly used in MATLAB, it plays a pivotal role in FIL simulations with MATLAB. Its key functions include FPGA design, creating HIL interfaces, enabling real-time processing, and facilitating co-simulation with MATLAB. Vivado is used to craft FPGA configurations and optimize logic designs. MATLAB communicates with FPGA hardware via Vivado-generated bitstream files, ensuring accurate real-time execution of control algorithms. Additionally, Vivado aids in co-simulation to validate FPGA components. Ultimately, Vivado seamlessly integrates MATLAB's control algorithms with FPGA hardware for precise and efficient real-time simulations and testing.

### 6.2.3 FIL-based controller implementation

The proposed control schemes for both boost and buck converters have undergone rigorous testing in a simulated environment, akin to the SIL technique. Having validated their performance in simulation, the next crucial step is to ensure that these control schemes operate correctly on a physical processor. This necessitates the use of the FIL technique. To verify the proposed control schemes using FIL, the control algorithm, previously implemented at the simulation level, needs to be transferred to an FPGA board, while the boost and buck converter models remain within the MATLAB/SIMULINK environment. This task is accomplished by leveraging MATLAB/SIMULINK in conjunction with an Artix 7 FPGA board.

In Figure 6.4, the depicted diagram provides a comprehensive representation of the proposed FIL technique [77]. This diagram serves to elucidate the organizational structure and functional relationships among various components involved in the FIL methodology. The visual representation highlights the intricate interplay between two fundamental domains: hardware, represented by the FPGA board, and software, encompassing MATLAB/SIMULINK. By showcasing these elements and their connections, the diagram elucidates the path of data and interactions within the FIL testing process. This visualization is instrumental in offering a clear and insightful perspective on the complex setup utilized for testing control strategy and converter models within the context of the FIL framework.

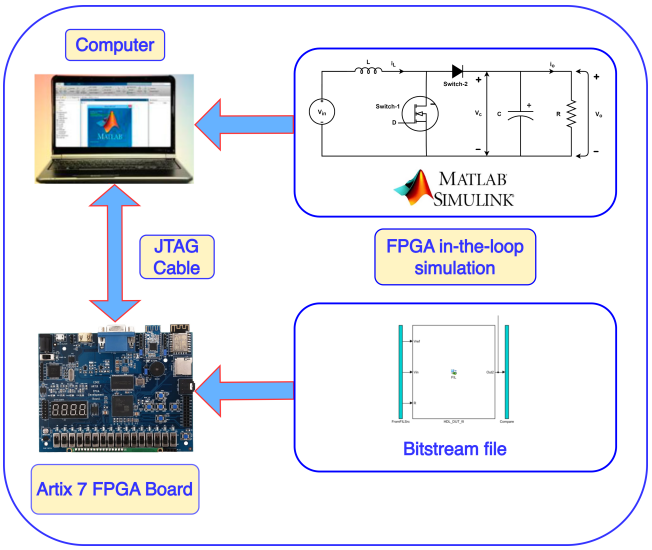



**Figure 6.4** Methodology of the performed FIL simulation

In summary, a detailed exploration of the FIL implementation process is presented. The focus is on the implementation of control algorithms, demonstrating the practical steps involved in this process. This section provides a comprehensive examination of the procedures and techniques used to achieve the implementation of controller algorithms within the FIL framework.

### 6.2.4 Challenges in Implementing the Controller in FIL Environment

In the realm of FIL simulations within the MATLAB/SIMULINK environment, the successful implementation of controllers presents a multitude of challenges. In this section, the challenges and complexities that can arise when control algorithms are integrated with FIL simulations will be discussed.

**HDL Coder library:** To validate control algorithms using FIL, it's important to understand the availability of blocks for HDL code generation. Within the HDL Coder library, some blocks are readily accessible and can be directly used in HDL code. These blocks are often designed and optimized for FPGA use, simplifying the implementation process. However, there may be instances where the specific blocks required for a particular control algorithm are not readily available. In such cases, custom logic must be created using the available HDL blocks. This custom logic design process involves combining and configuring existing HDL blocks to fulfill the algorithm's requirements.

**Numerical precision and scaling:** In a continuous environment, such as mathematical modeling in control systems, mathematical abstractions are often employed, assuming infinite precision. In this idealized setting, physical quantities like voltage or current are represented as real numbers with infinite decimal places, allowing for accurate mathematical operations and comparisons.

However, in the FIL environment, where hardware, particularly FPGAs, is utilized, a fundamentally different approach is taken. FPGAs are hardware devices with limited numerical precision compared to software simulations. They operate on digital logic and finite-precision representations, typically employing fixed-point or integer arithmetic. Consequently, continuous signals, such as voltage or current, must undergo conversion into discrete, integer-based representations to be effectively processed on the FPGA.

During the conversion of continuous signals into fixed-point or integer representations, inherent precision is sacrificed. For example, when representing voltage as a fixed-point number, there is a limited number of bits available for both the integer and fractional parts. If this process is not meticulously executed, the loss of precision can introduce errors in computational outcomes.

However, while converting data types, it's imperative to strike a balance between precision and efficiency. Optimizing data type conversion is essential for minimizing program size, conserving memory, and reducing computation time. Choosing the most suitable data type, often one with the lowest precision that still meets accuracy requirements, can significantly impact resource utilization. This is especially critical in resource-constrained environments

like embedded systems or FPGA-based applications, where efficient memory allocation and computation are paramount. Careful consideration of data type conversions ensures that computational resources are used judiciously, enhancing both the performance and resource efficiency of the program.

Moreover, to prevent the loss of precision, it is essential to implement appropriate data scaling techniques. Scaling means multiplying signals by the right numbers to make them larger without changing their fractional parts. However, it's crucial to apply this scaling carefully in every aspect of the control algorithm, including multiplication and division operations. Failure to do so can lead to inaccurate data comparisons. In FPGA-based control systems, these data comparisons play a pivotal role in making control decisions. Mishandling the scaling process can lead to situations where two signals that should be equivalent in the continuous domain do not appear equal in the discrete representation used by the FPGA. Consequently, this discrepancy can result in incorrect control actions being taken.

**Synchronization:** Synchronization is the process of ensuring that all signals in the control system are aligned in time. In FIL simulations, the FPGA interacts with other components, such as sensors, actuators, and software models, which may run on different clock domains. Proper synchronization ensures that data exchanges occur at the right time and are correctly interpreted by all components. If signals are not synchronized, it can lead to misinterpretation of data, resulting in control errors or instability. For example, if the FPGA receives sensor data at an inconsistent rate, it might misinterpret the timing of control decisions.

**Managing time constraints:** Validating every step of the HDL Workflow Advisor to generate a Bitstream file is a time-consuming but essential task in FIL simulations. This process, which involves configuring FPGA design settings, checking for design compliance with constraints, and synthesizing the design, can vary in duration from a few minutes to several hours. The time required depends on factors like the processing power of the computer and the complexity of the control algorithm being implemented. Once the Bitstream file is successfully generated, it's not the end of the process. Deploying the Bitstream onto the FPGA can also take a few minutes. However, the work doesn't stop there. Continuous validation is necessary, as any discrepancies or errors found during FIL simulations may necessitate adjustments. This iterative process of validation, modification, and repetition contributes to the overall time-consuming nature of FPGA development for FIL applications. Despite its time intensity, this meticulous approach is essential to ensure the reliability and correctness of FPGA-based control systems.

In conclusion, when these considerations are managed attentively, the control algorithm can be effectively validated using FIL simulations. This complete testing not only confirms the algorithm's feasibility but also builds confidence in its performance and reliability when

deployed in real-world control systems. By meticulously managing data types, accurately scaling signals, and adhering to the workflow, the desired objectives can be met, and robust functionality in practical applications can be ensured for FPGA-based control systems.

## 6.3 FIL-Based Analysis of the Proposed Scheme for Boost Converter

A comprehensive performance evaluation and behavior of the proposed scheme is carried out within the FIL simulation environment. The Fig. 6.5 illustrates the experimental configuration employed to evaluate the open-loop behavior of a boost converter during ongoing FIL simulation. It shows the tools used, like the Artix 7 FPGA board and MATLAB/SIMULINK software, to study how the converter behaves in different situations. This arrangement is essential for acquiring data and insights into the performance of the control algorithm using FIL, offering valuable information for validating and optimizing control strategies.

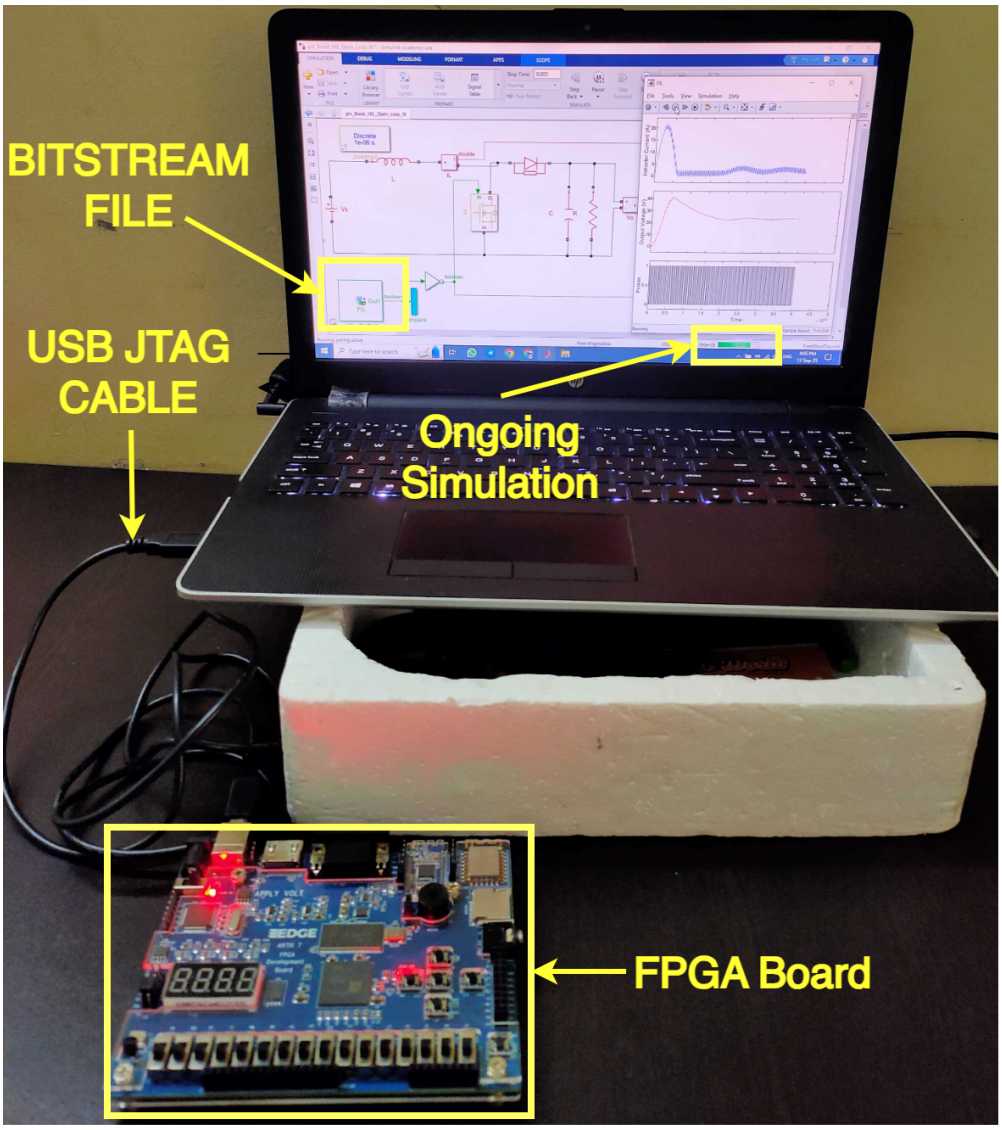
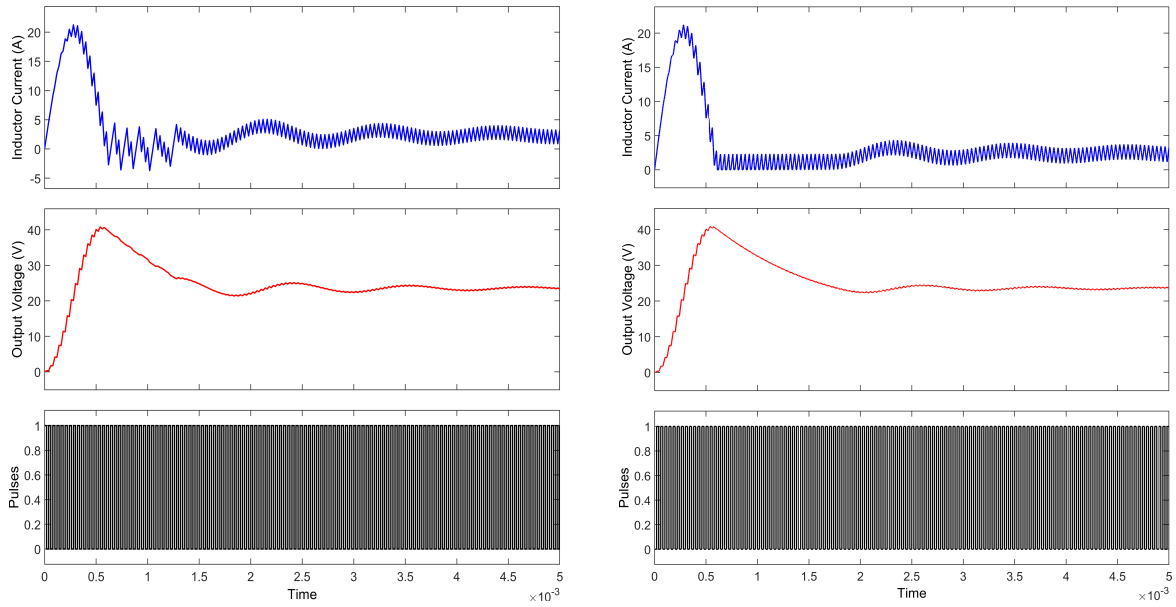



**Figure 6.5** Experimental setup for open-loop response evaluation of boost converter using FIL

### 6.3.1 Comparative open-loop analysis: Simulation vs. FIL environment

The open-loop behavior of the boost converter is analyzed in both the SIMULINK and FIL environments, and the outcomes are illustrated in Figure 6.6a and Fig. 6.6b, respectively. For this analysis, the boost converter's nominal parameters are considered, as previously detailed in Chapter 3, with a 50% duty cycle. The steady-state behavior is quite similar in both environments, suggesting consistency under stable conditions. However, slight differences arise in the transient response, likely due to FIL's discrete modeling, contrasting SIMULINK's continuous mathematical functions. FIL's discrete time steps can introduce these minor transient variations while maintaining overall steady-state similarity.

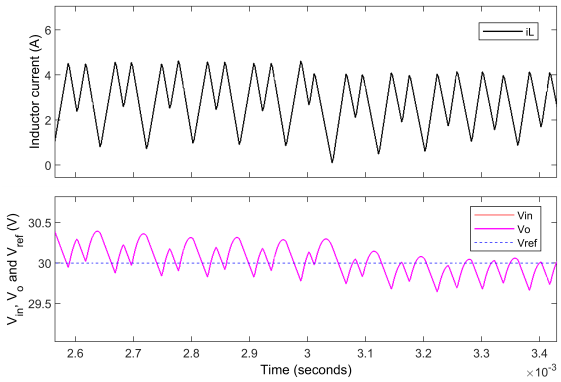



**(a)** SIMULINK environment **(b)** FIL environment

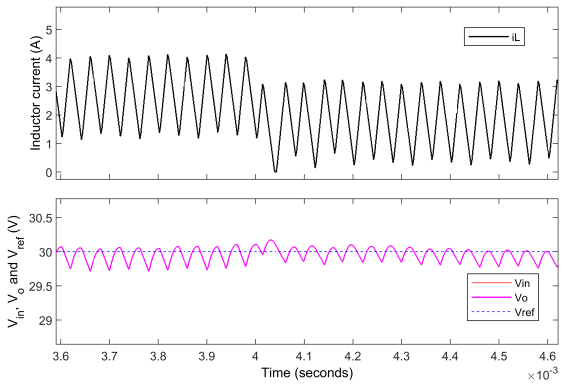
**Figure 6.6** Open-loop response of the boost converter

### 6.3.2 CCM behavior in FIL

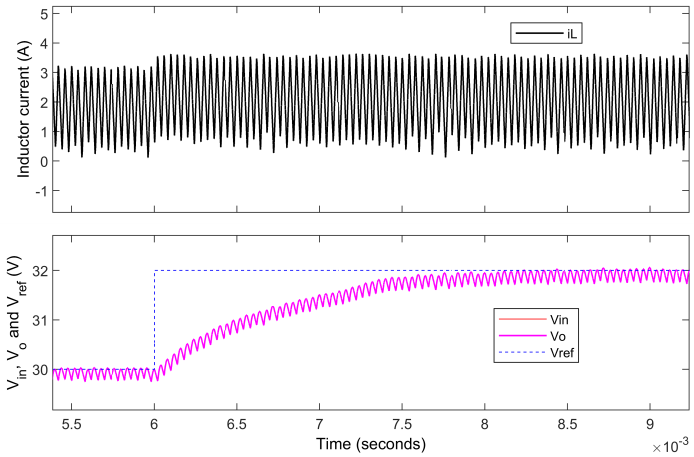
Various changes in line, load, and set-point conditions are introduced to ensure a comprehensive and rigorous testing of the controller in the FIL environment. At $t$ = 3 ms, a line variation of 2 V is introduced, resulting in $V_{in}$ = 17 V. The controller adeptly manages this change, maintaining a stable output voltage, as demonstrated in Fig. 6.7a. Subsequently, at $t$ = 4 ms, a load variation is introduced by adding an additional 10 Ω to the load, resulting in a total resistance of 30 Ω. The controller effectively handles this load variation, as evidenced in Fig. 6.7b. Furthermore, set-point tracking is evaluated at $t$ = 6 ms, with $V_{ref}$ set to 32 V as shown in Fig. 6.7c. Remarkably, within 3 ms, the controller settles at the new set-point.




**(a)** Step-up change in $V_{in}$ from 15 V to 17 V at $t$ = 3 ms




**(b)** Step-up change in $R$ from 20 Ω to 30 Ω at $t$ = 4 ms



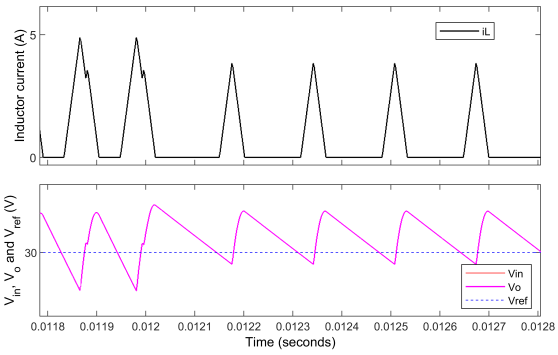

**(c)** Step-up change in $V_{ref}$ from 30 V to 32 V at $t$ = 6 ms

**Figure 6.7** CCM analysis of boost converter with the proposed scheme in FIL environment

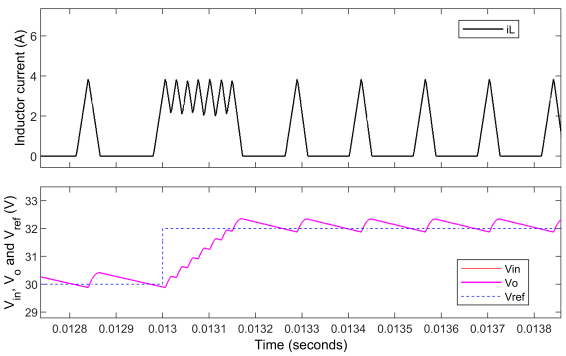
Collectively, these results validate the performance of the controller implementation during CCM in the FIL environment.

### 6.3.3 DCM behavior in FIL

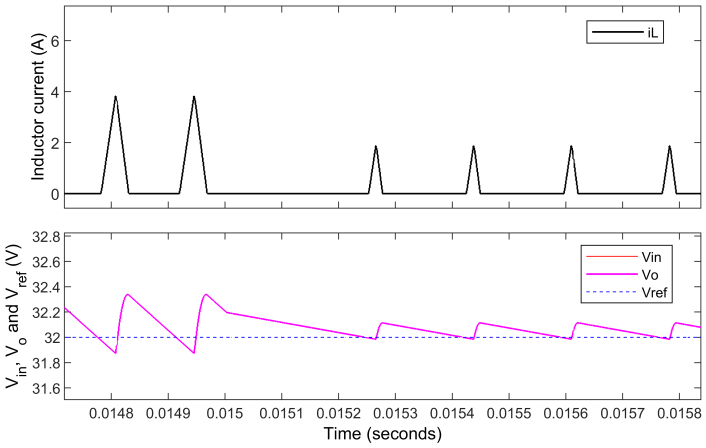
Similar to the CCM scenario, in DCM as well, various disturbances are applied to assess the controller's performance in the FIL environment. At $t$ = 12 ms, the load is increased to 100Ω, as depicted in Fig. 6.8a. It is evident from the figure that the output voltage remains stable under this load condition. Furthermore, at $t$ = 13 ms, the set-point is changed from 30 V to 32 V. The controller promptly responds to this set-point change, and the output effortlessly tracks the new reference voltage, as illustrated in Fig. 6.8b. Additionally, while the set-point is at 32 V, the load is further increased to 500 Ω. Remarkably, the output voltage remains quite stable under this higher load condition, as shown in Fig. 6.8c. These results show that the controller works well in the FIL environment, even when the system operates in DCM. This proves that the controller is reliable and effective in this particular setup.




**(a)** Step-up change in $R$ from 37.7 Ω to 100 Ω at $t$ = 12 ms




**(b)** Step-up change in $R$ from 30 V to 32 V at $t$ = 13 ms




**(c)** Step-up change in $R$ from 100 Ω to 500 Ω at $t$ = 15 ms

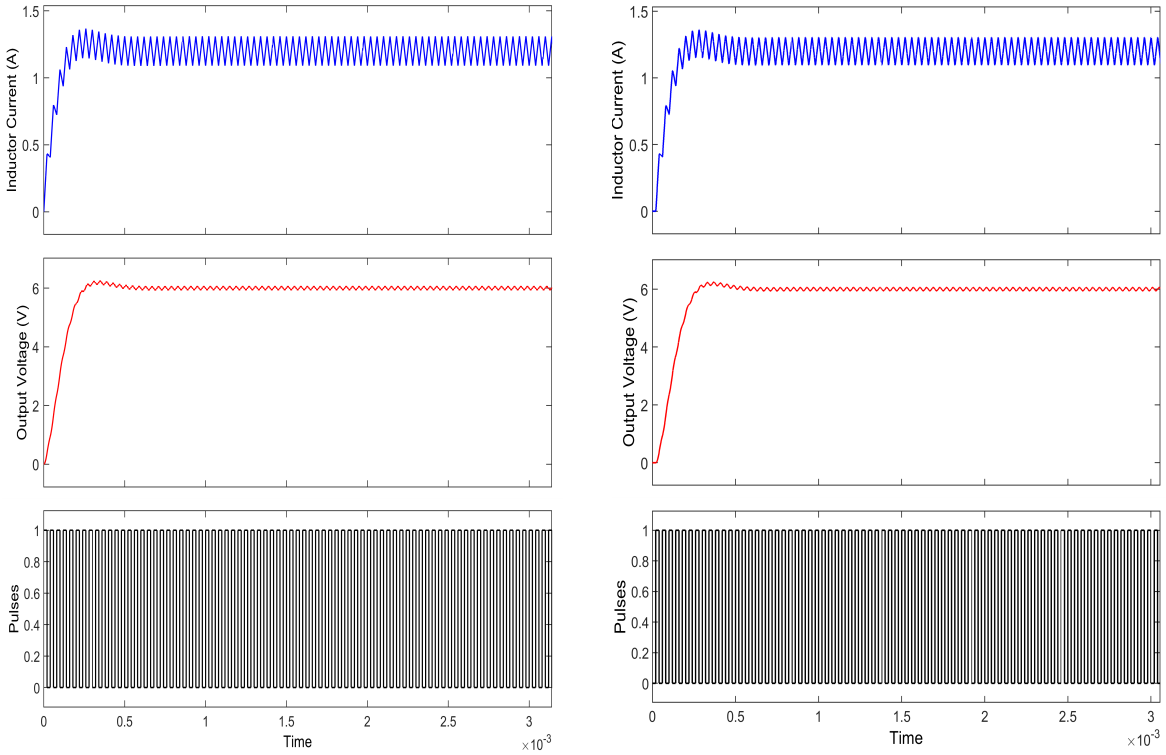
**Figure 6.8** DCM analysis of boost converter with the proposed scheme in FIL environment

## 6.4 FIL-Based Analysis of the Proposed Scheme for Buck Converter

The proposed control scheme is rigorously analyzed using a FIL approach for the buck converter. Through this FPGA-based analysis, the scheme's effectiveness, real-time performance, and suitability for practical implementation are thoroughly evaluated, providing valuable insights for its application in power electronics systems.

### 6.4.1 Comparative open-loop analysis: Simulation vs. FIL environment

The open-loop analysis of the buck converter is conducted in a manner consistent with the approach used for the boost converter. This involves examining the behavior of the buck converter within both simulation and FIL environments. In this examination, the standard parameters of the buck converter, as outlined in Table 4.2, are taken into account while maintaining a duty cycle of 50%. The resemblance between steady-state and transient behaviors in both environments indicates a consistent response under stable conditions, as illustrated in Fig. 6.9.



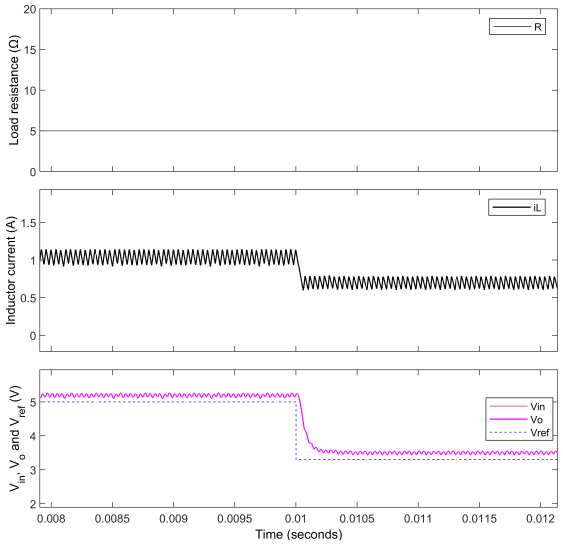

**(a)** SIMULINK environment **(b)** FIL environment

**Figure 6.9** Open-loop response of the buck converter

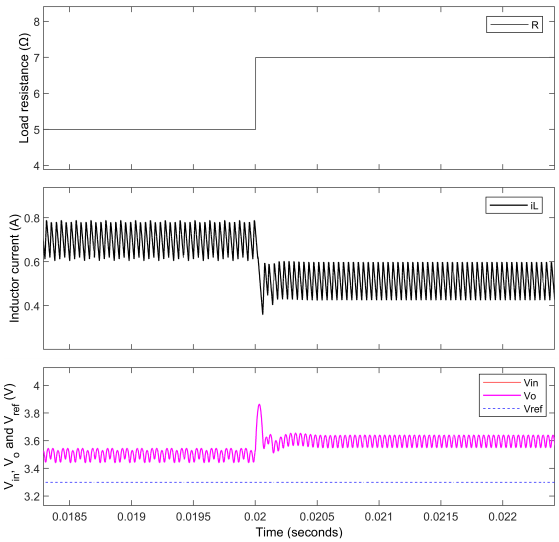
### 6.4.2 CCM behavior in FIL

A variety of alterations in line voltage, load characteristics, and set-point values are implemented to guarantee thorough and extensive testing of the controller within the FIL environment as depicted in Fig. 6.10. In the regulatory evaluation, various tests are conducted on the controller's performance. Firstly, at $t = 0.01$ seconds, set-point tracking is examined, as indicated in Fig. 6.10a. Despite the controller successfully tracking the set-point, the output voltage exhibits a slight elevation. Subsequently, load disturbances are introduced at $t = 0.02$ seconds and $t = 0.05$ seconds, as displayed in Fig. 6.10b and 6.10d , respectively. Similar to the set-point test, the output voltage registers a minor increase during load changes. Furthermore, a line voltage variation is tested at $t = 0.03$ seconds, as shown in Fig. 6.10c, where once again, the output voltage slightly exceeds the reference.

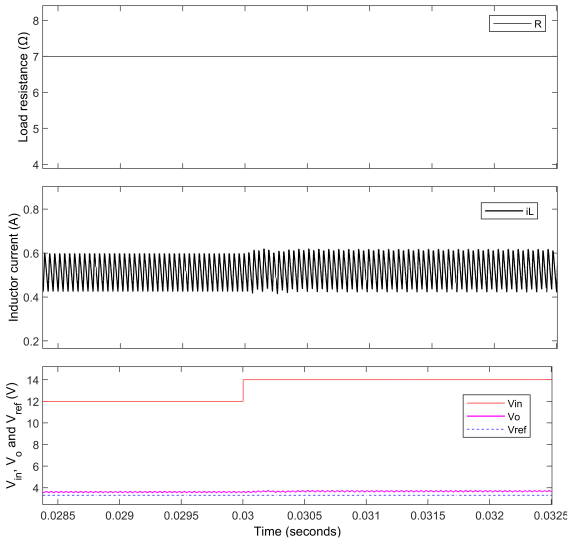
This consistent phenomenon of the output voltage being slightly higher in all cases can be attributed to scaling and conversion factors, resulting in this marginal deviation. Despite these minor deviations, the controller implementation showcases stability and effectiveness for the buck converter with the proposed scheme, demonstrating its robust performance in the FIL environment.



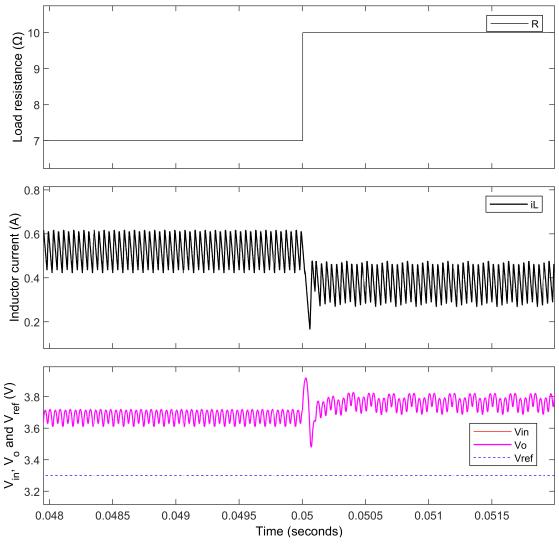

**(a)** Step-down change in $V_{ref}$ from 5 V to 3.3 V at $t$ = 0.01 sec




**(b)** Step-up change in $R$ from 5 Ω to 7 Ω at $t$ = 0.02 sec




**(c)** Step-up change in $V_{in}$ from 12 V to 14 V at $t$ = 0.03 sec




**(d)** Step-up change in $R$ from 7 Ω to 10 Ω at $t$ = 0.05 sec

**Figure 6.10** CCM analysis of buck converter with the proposed scheme in FIL environment

## 6.5 Comparative Analysis

The significance of the comparative analysis of the FIL technique lies in its ability to evaluate performance, efficiency, and adaptability across various platforms and scenarios. This assessment aids in the identification of strengths and weaknesses, guiding optimization and ensuring suitability for a wide range of real-time control applications. Ultimately, enhanced system reliability and performance in practical implementations are achieved through this process.

### 6.5.1 Comparative analysis based on implementation technique

A comprehensive comparative analysis is undertaken, with a focus on the implementation techniques employed for the study. A novel parametrizable fixed-point arithmetic forFPGAs was introduced, enabling flexible point adjustments without model redesign. It efficiently models a buck converter with <20 ns simulation. The model adapts to various values, maintaining accuracy without resynthesis, showcasing superiority over fixed-point arithmetic [99]. The Controller HIL (CHIL) lab allowed for the design, control, and testing of power converters without worrying about component failure. The CHIL setup allowed the physical controller to be directly validated, eliminating the need for real power converters. This resulted in more repeatable results and enabled extreme digital controller testing of power converters that were previously impossible with real hardware [100]. The second-order boost converter's NMP behavior is tackled through the utilization of a 2 Degree of Freedom (DOF)-PID controller, which is then implemented on an FPGA platform [101]. A proposal for robust velocity control of a DC motor using parallel DC-DC buck converters and generalized PI-observers-based ADRC is made, with theoretical calculations being validated through FPGA-based implementation [102]. Thus, distinct methodologies and approaches are closely scrutinized, with attention given to the controller implementation methods between these techniques, as shown in Table 6.1. Here, [99], [101], and [102] employed FPGA for controller realization, while [100] utilized NI-MyRIO. All these methods adopted the HIL/FIL MBD approach. The aim of this analysis is to provide valuable insights into the practical applicability of the proposed control strategies in FPGA-based control systems.

**Table 6.1** Diverse approaches to controller realization

| Proposal | Converter | Modeling/ Controller | Controller Realization | Plant Realization | MBD Approach |
|---|---|---|---|---|---|
| [99] | Buck | State-space | Xilinx FPGA Zynq 7 | MATLAB/ SIMULINK | HIL/FIL |
| [100] | Boost | PI | NI-MyRIO | NI PXIe-FPGA | HIL |
| [101] | Boost | PID | Xilinx FPGA Zynq 7 | MATLAB/SIMULINK | HIL/FIL |
| [102] | Buck | ADRC | Xilinx FPGA Artix 7 | Hardware | HIL |
| Proposed | Buck | SDS/BC | Xilinx FPGA Artix 7 | MATLAB/SIMULINK | FIL |
| Proposed | Boost | SDS/BC | Xilinx FPGA Artix 7 | MATLAB/SIMULINK | FIL |

Thus, thorough comparative analysis delves into the intricacies of various methodologies, with particular emphasis on their unique approaches to controller realization. This scrutiny illuminates the practical feasibility and promise of the proposed control strategies within the realm of FPGA-based control systems. This investigation not only contributes to the

understanding of these techniques but also guides future research and application in the field of control systems.

### 6.5.2 Comparative analysis based on FPGA resource utilization

Table 6.2 displays the FPGA resource allocation associated with the proposed scheme for both boost and buck converters. For the boost converter, the proposed scheme consumes 0.242 W of on-chip power, whereas for the buck converter, the corresponding figure is 0.206 W. The resource usage in boost converter control strategy is slightly greater compared to buck converter control. This is because the boost converter controller is designed for both CCM and DCM, whereas the buck converter controller is designed solely for CCM operation.

**Table 6.2** Resource utilization breakdown for FPGA in proposed controller implementation

| Proposed Schemes → | | Boost Converter | | Buck Converter | |
|---|---|---|---|---|---|
| Resource | Available | Utilization | Utilization % | Utilization | Utilization % |
| LUT | 20800 | 7778 | 37.39 | 2927 | 14.07 |
| LUTRAM | 9600 | 113 | 1.18 | 23 | 0.24 |
| FF | 41600 | 4484 | 10.78 | 1262 | 3.03 |
| BRAM | 50 | 4 | 8.00 | 4 | 8.00 |
| DSP | 90 | 31 | 34.44 | 2 | 2.22 |
| IO | 170 | 1 | 0.59 | 1 | 0.59 |
| BUFG | 32 | 3 | 9.38 | 3 | 9.38 |
| MMCM | 5 | 1 | 20.00 | 1 | 20.00 |

A novel approach is introduced for complex system design, streamlining design tasks and expediting the transition from system modeling to hardware implementation. To assess the platform's development, a practical case study is conducted involving a controlled power converter, with FPGA implementation of the digital controller [74]. Additionally, a new error-based ADRC (eADRC) is derived from a standard PI/PID controller and a series of tests are performed to validate the findings. A comparative analysis is conducted in FIL simulation using a realistic plant model of a buck converter [103]. However, when applying controllers to the buck converter, the primary focus remains solely on comparing the control algorithms, preserving the original context. Thus, the proposed approaches are assessed against both the traditional PID scheme and state-of-the-art techniques such as eADRC. This evaluation focuses on determining the FPGA resources necessary for implementing these controllers. Table 6.3 offers a succinct overview of the utilization of FPGA resources by the proposed scheme in comparison to other schemes.

**Table 6.3** FPGA resource allocation comparison in various schemes

| Proposal | PID [74] | | eADRC [103] | | | Proposed scheme | | | Proposed scheme | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Converter | Buck | | Buck | | | Buck | | | Boost | | |
| Mode | Not specified | | Not specified | | | CCM | | | CCM + DCM | | |
| FPGA Board | Xilinx Spartan 6 | | Xilinx Artix 7 | | | Xilinx Artix 7 | | | Xilinx Artix 7 | | |
| FPGA Resource | LUTs | DSP blocks | LUTs | FFs | DSP blocks | LUTs | FFs | DSP blocks | LUTs | FFs | DSP blocks |
| Available Resources | 5720 (100%) | 16 (100%) | 20800 (100%) | 41600 (100%) | 90 (100%) | 20800 (100%) | 41600 (100%) | 90 (100%) | 20800 (100%) | 41600 (100%) | 90 (100%) |
| Utilized Resources | 931 (16.2%) | 12 (75%) | 1005 (4.83%) | 216 (0.52%) | 52 (57.78%) | 2927 (14.07%) | 1262 (3.03%) | 2 (2.22%) | 7778 (37.39%) | 4484 (10.78%) | 31 (34.44%) |

A comparative examination between the novel scheme for buck converter control and the traditional PID approach [74] highlights a significant disparity in the utilization of FPGA resources. The analysis underscores that the proposed schemes demonstrate more efficient resource utilization, necessitating fewer Lookup Tables (LUTs), Flip Flops (FFs), and Digital Signal Processing (DSP) blocks for their controller implementations in the context of the buck converter. The increased resource consumption observed in the proposed boost converter scheme, in contrast to the buck converter, stems from its dual-mode design, which accommodates both CCM and DCM operations.

On the other hand, When comparing eADRC [103] to the proposed schemes tailored for both converters, it becomes apparent that eADRC requires fewer resources in terms of LUTs and FFs. However, it's noteworthy that the utilization of DSP blocks is notably higher in the case of eADRC when compared with the proposed schemes. This increased utilization of DSP blocks suggests that eADRC likely employs a more intricate algorithm compared to the proposed schemes. The advantage of the proposed schemes lies in their capacity to achieve minimal mathematical computations, as evidenced by their reduced usage of DSP blocks. This trade-off in resource utilization provides insight into the relative computational complexity and efficiency of these control techniques within the context of FPGA implementation. Such observations underscore the importance of selecting an appropriate control strategy based on the available FPGA resources and desired performance metrics.

## 6.6 Summary

An overview of various MBD approaches is provided, highlighting their respective advantages. Detailed steps for implementing the controller in FPGA, utilizing FIL in conjunction with MATLAB/SIMULINK, are presented. The validation of the proposed schemes for both boost

and buck converters is accomplished through the FIL approach. Additionally, a comparative analysis is conducted, contrasting the proposed schemes with both conventional and advanced techniques. Furthermore, techniques employed by other researchers for controller realization are explored, adding to the comprehensive examination of the field.

# CHAPTER-7

# Conclusion and Future Scope

## 7.1 Conclusion

In this research, the primary focus centers on addressing the complexities and challenges inherent in the control of dynamic systems undergoing mode transitions, particularly within the domain of boost and buck converters. These converters' models are characterized as SDS utilizing hybrid automaton representation, which factors in mode-dependent parameters. This approach results in a more precise depiction of the systems' dynamics.

The control algorithm proposed in this study exhibits remarkable robustness in effectively managing mode transitions. It ensures stability, convergence, and the attainment of desired performance objectives during the execution of switching operations. To verify the stability properties of the system, a rigorous stability analysis is conducted using the Lyapunov method, which definitively establishes its stability.

Confirmation of the control system's practical applicability is achieved through the successful implementation using the FIL technique on the Xilinx Artix 7 FPGA board. This action not only serves to validate its functionality but also contributes to the system's adaptability and design flexibility.

Comprehensive performance evaluations, conducted in a comparative manner, undeniably reveal the superiority of the proposed control algorithm when compared to conventional methods and state-of-the-art techniques.

This research marks a significant milestone in advancing the understanding and effectiveness of control strategies for SDS. The knowledge and insights gained through this study hold practical applicability across diverse domains characterized by complex dynamic systems, with a particular focus on the domain of boost and buck converters.

## 7.2 Future Scope

The path forward offers exciting possibilities for advancing the field. Future endeavors can delve into the exploration of cutting-edge FPGA platforms and innovative design methodologies. By harnessing these advanced resources, the implementation of the proposed control algorithm can be further refined and optimized. This evolution holds the potential to yield control systems that are not only highly efficient but also remarkably resource-friendly. Such advancements not only contribute to the field of control theory but also hold the promise of practical, sustainable solutions in various applications, from power electronics to cyber-physical systems.

Investigating control strategies for SDS within multi-agent systems, where multiple SDS entities interact, presents captivating research prospects. This inquiry holds immense potential for applications such as swarm robotics and autonomous vehicles, where coordinated, adaptive control is essential for achieving collective goals and navigating complex environments effectively.

Transferring the insights acquired through this research to diverse domains characterized by intricate dynamic systems holds substantial promise. In aerospace, the application of advanced control strategies can lead to more efficient and agile flight systems. Similarly, in the realm of biomedical devices, these insights can contribute to enhanced patient care and medical technology. Moreover, within industrial automation, the optimization of control techniques can drive productivity and efficiency gains, paving the way for innovative solutions across these sectors.

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# List of Publications

## Published Paper

- Hardik Patel and Ankit Shah, “Boundary-based hybrid control algorithm for switched boost converter operating in ccm and dcm,” International Journal of Electrical and Electronics Research, vol. 11, no. 1, pp. 213–221, 2023. DOI: https://ijeer.forexjournal.co.in/ archive/volume-11/ijeer-110129.html. (Scopus Indexed).

- Hardik Patel and Ankit Shah, “Boundary-based pwm control scheme for a dc-dc buck converter operating in ccm,” Transactions on Energy Systems and Engineering Applications, vol. 4, no. 1, pp. 1–17, 2023. DOI: https://doi.org/10.32397/tesea.vol4.n1.504. (Scopus Indexed).

## Communicated Paper

- Hardik Patel and Ankit Shah, "Lyapunov Stability Analysis and FIL Implementation for Boundary-Based Hybrid Controller in Boost Converter," Advanced Control for Applications. (Scopus Indexed)

- Hardik Patel and Ankit Shah, "Stability Analysis of Boundary-Based Controller for Buck Converter and FIL Implementation," International Journal of Computing and Digital Systems. (Scopus Indexed)